UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2012/2013

COURSE NAME	:	DIGITAL ELECTRONICS
COURSE CODE	:	BEL 20303 / BEX 21103 / BEE 2233
PROGRAMME	:	BEE/BEB/BEC/BED/BEH/BEU
EXAMINATION DATE	:	JANUARY 2013
DURATION	:	2 HOURS 30 MINUTES
INSTRUCTION	:	1. ANSWER **ALL** QUESTIONS 2. ATTACH **APPENDIX I, II AND III** WITH YOUR ANSWER BOOKLET

THIS QUESTION PAPER CONSISTS OF **ELEVEN (11)** PAGES

Q1 (a) Explain the differences between sum-of-product and product-of-sum expression.

(4 marks)

(b) Simplify the following Boolean expression.

(i) $\overline{A \cdot \overline{(B + \overline{C})} \cdot D}$

(2 marks)

(ii) $(X + Z)(\overline{X} + Y)$

(4 marks)

(c) Prove the following Boolean expression

$$\overline{B} \cdot C + C \cdot \overline{D} + A \cdot \overline{D} + \overline{A} \cdot B \cdot \overline{C} \cdot D = (A + B + C) \cdot (A + C + D) \cdot (\overline{B} + \overline{C} + \overline{D}) \cdot (\overline{A} + C + \overline{D})$$

(5 marks)

Q2 (a) Explain the difference between serial data transmission and parallel data transmission.

(4 marks)

(b) **Figure Q2** shows a parity generator circuit using multiplexer. Analyze the operation of this circuit and state the type of parity method realized by this circuit.

(11 marks)

Q3 (a) Design a four-line to two-line priority encoder circuit with active HIGH inputs and outputs, with priority assigned to the higher-order data input line.

(7 marks)

(b) The waveforms for signals A and B shown in **Figure Q3(b)(i)** are applied to the circuit shown in **Figure Q3(b)(ii)**. Evaluate the waveforms for P, Q, R and S in the **APPENDIX I**. Assumes that initially R=0 and S=1.

(4 marks)

(c) A 4-bit shift register constructed from edge-triggered D-type flip flops is shown in **Figure Q3(c)**. If, on successive rising edges of the clock signal CLK, the input takes on the values 1 0 1 0 1 1 1 0, what are the contents of the shift register after each edge of the clock? You may assume that the register contains all zeroes initially.

(4 marks)

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Q4 (a) **Figure Q4(a)** shows a 4-bit counter with a specific MOD. MR input is used to reset all flip-flop to LOW. Sketch the timing diagram for Q0, Q1, Q2, Q3, X and Y in the **APPENDIX II**.

(6 marks)

(b) **Figure Q4(b)** shows the circuit of a state machine with extra input X. It consists of D flip-flop, J-K flip-flop and two gates. Assume that the initial values of A and B are zero, draw the state transition diagram for this state machine.

(9 marks)

Q5 Tyrone Shoelaces has invested a huge amount of money into the stock market and does not trust just anyone to give him buying and selling information. Before he will buy a certain stock, he must get input from three sources. His first source is Pain Webster, a famous stock broker. His second source is Meg A. Cash, a self-made millionaire in the stock market, and his third source is Madame LaZora, a world-famous psychic. After several months of receiving advice from all three, he has come to the following conclusions:

- Buy if Pain and Meg both say yes and the psychic says no.
- Buy if the psychic says yes.
- Do not buy otherwise.

(a) Construct a truth table and find the minimized Boolean function to implement the logic telling Tyrone when to buy

(10 marks)

(b) Design the logic circuit to realize the logic system in Q5(a)

(4 marks)

(c) Implement the circuit obtained in Q5(b) using two inputs NAND gate only with minimal number of gates.

(6 marks)

Q6 (a) Circuit in **Figure Q6(a)(i)** has three inputs (A, B and C) and one output (Z). Construct the truth table. Refer **Figure Q6(a)(ii)** datasheet for pin assignment.

(10 marks)

(b) Based on truth table you obtained in Q6(a), implement the circuit using multiplexer in **Figure Q6(b)(i)** (please answer in **APPENDIX III**). Show all connection. Refer to **Figure Q6(b)(ii)** for datasheet pin assignment.
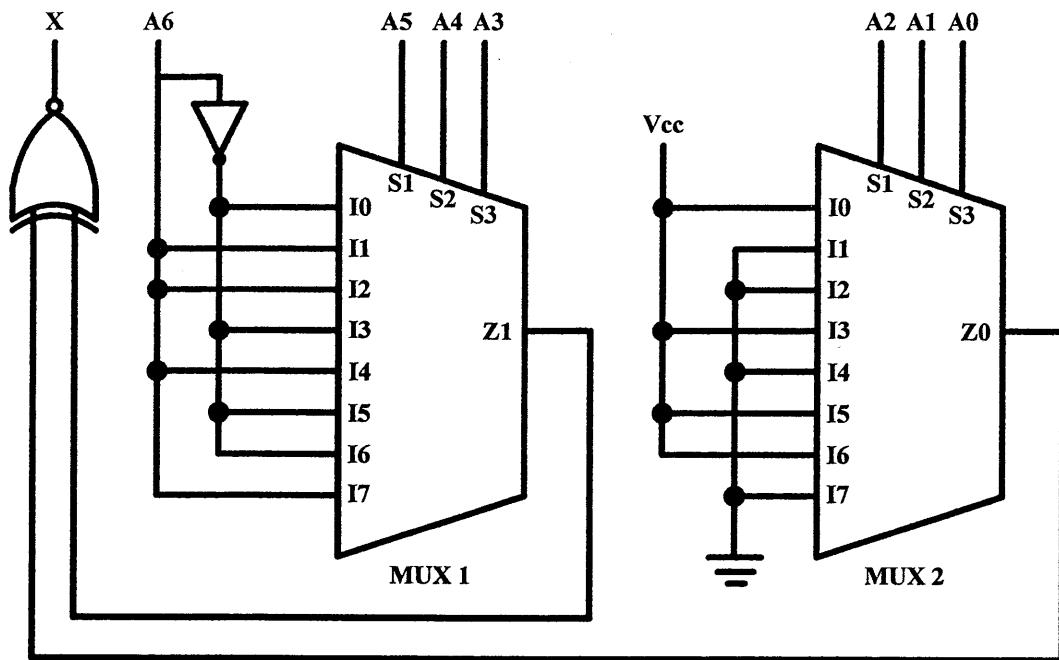
(10 marks)

- END OF QUESTION -

FIGURE Q2

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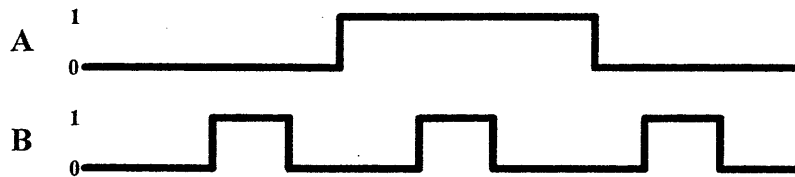COURSE :DIGITAL ELECTRONICS   COURSE CODE :BEL20303/BEX21103/BEE2233
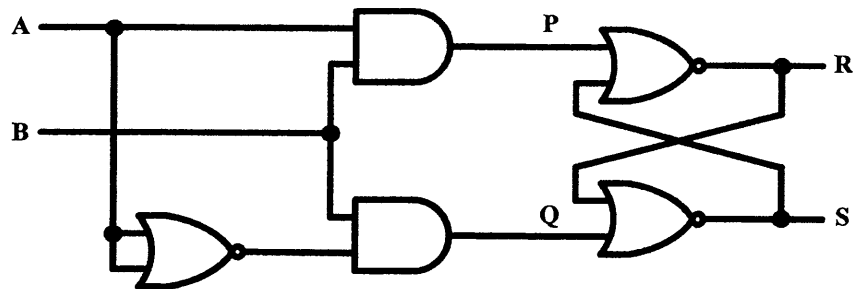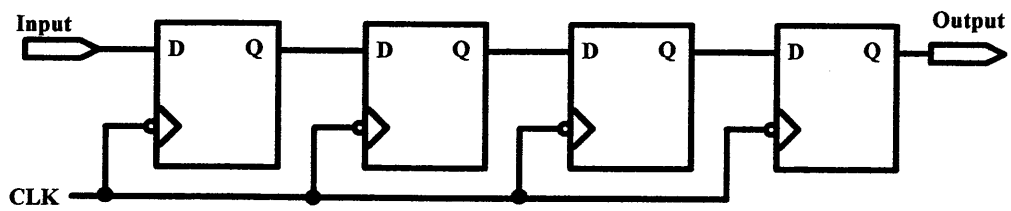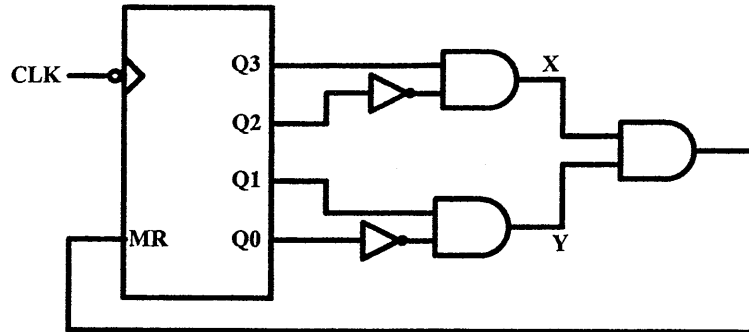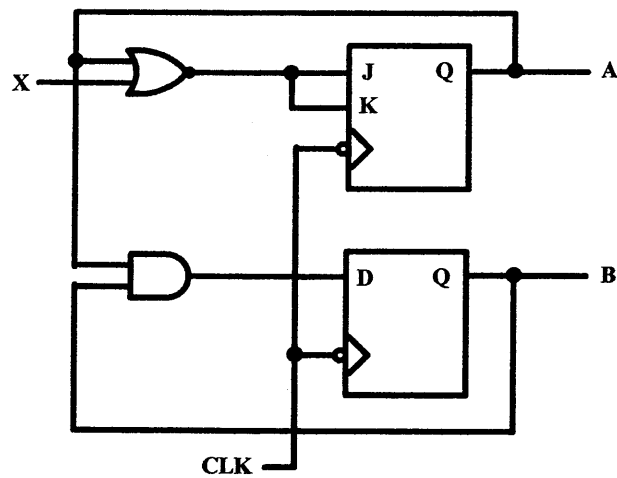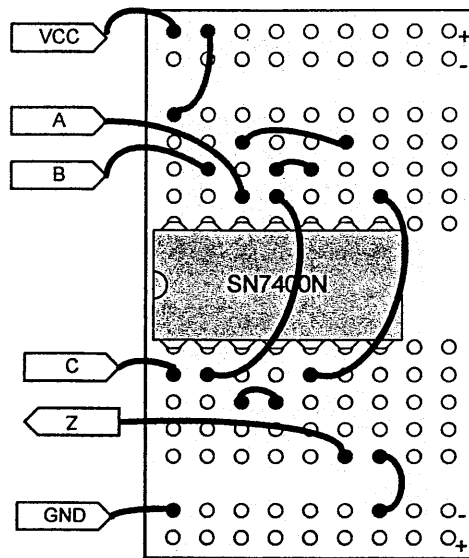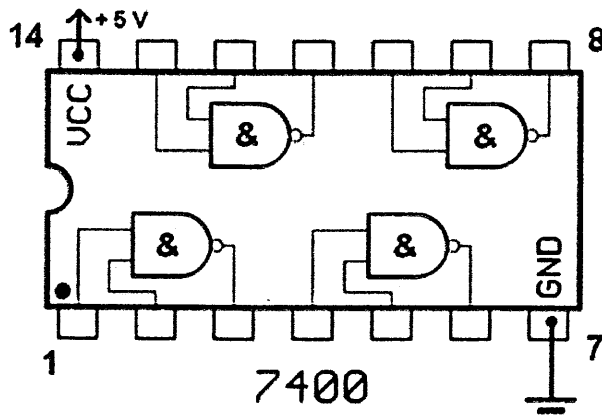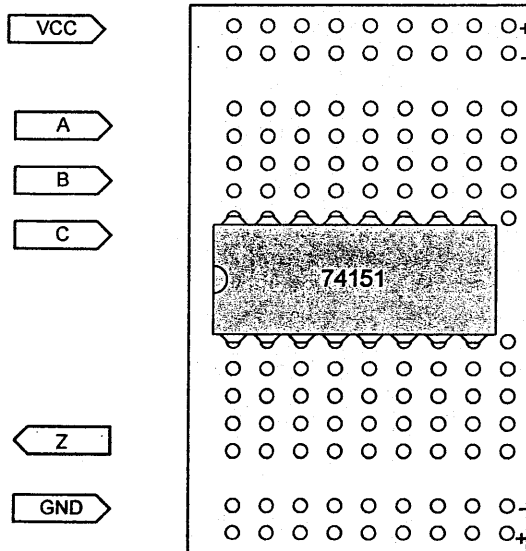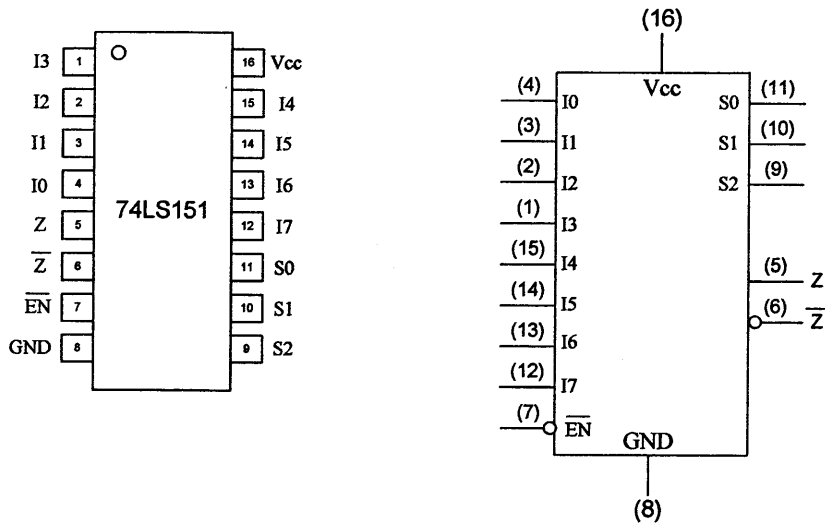

FIGURE Q3(a)(i)

FIGURE Q3(a)(ii)

FIGURE Q3(c)

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FIGURE Q4(a)

FIGURE Q4(b)

FIGURE Q6(a)(i)

FIGURE Q6(a)(ii)

FIGURE Q6(b)(i)

FIGURE Q6(b)(ii)

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APPENDIX I

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APPENDIX II

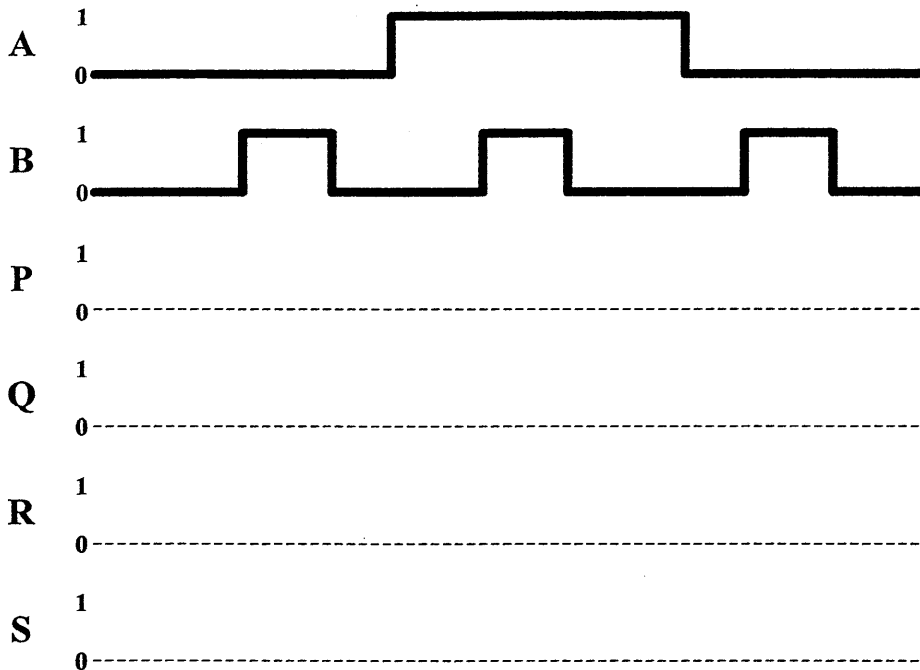# FINAL EXAMINATION

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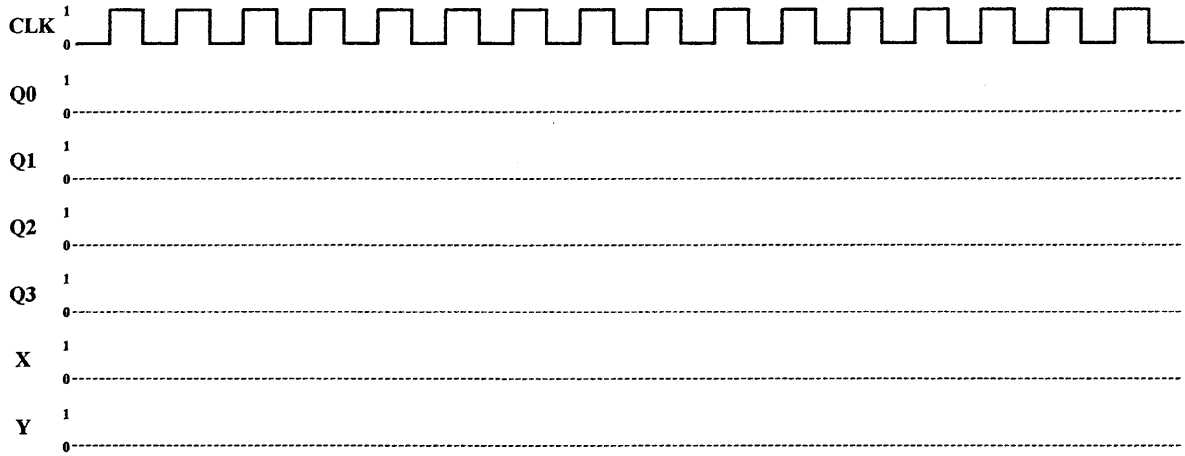COURSE   :DIGITAL ELECTRONICS   COURSE CODE   :BEL20303/BEX21103/BEE2233

APPENDIX III