

CONFIDENTIAL



UNIVERSITI TUN HUSSEIN ONN MALAYSIA

**FINAL EXAMINATION
SEMESTER II
SESSION 2018/2019**

COURSE NAME : ELECTRICAL AND ELECTRONIC TECHNOLOGY

COURSE CODE : BDA 14303

PROGRAMME CODE : BDD

EXAMINATION DATE : JUNE/JULY 2019

DURATION : 3 HOURS

INSTRUCTION : PART A: ANSWER ONE(1) QUESTION ONLY
PART B: ANSWER ALL QUESTIONS

THIS QUESTION PAPER CONSISTS OF **THIRTEEN (13)** PAGES

TERBUKA
CONFIDENTIAL

PART A:

- Q1** (a) Explain the function of the following component:
- (i) Digital multi-meter (2 marks)
 - (ii) Variable resistors (2 marks)
- (b) In a closed loop series circuit, it consists of voltage sources 12V, three (3) resistors: R1 (1200m Ω), R2 (550 Ω) and R3 (1.2k Ω). Determine the current (I), and the power in R1, R2 and R3. (5 marks)
- (c) Referring to **Figure Q1(c)**, calculate the total resistance (R_T) of the circuit. (6 marks)
- (d) Given **Figure Q1(d)**, using Wye-Delta Transformation to determine the total resistance, R_T and the current I, if the given voltage in this circuit is 15V. (10 marks)
- Q2** (a) Define the Norton Theorem. (4 marks)
- (b) Referring to **Figure Q2(b)**, solve the Norton equivalent circuit for the circuit at terminal a-b. (6 marks)
- (c) Evaluate the v_o in the circuit of **Figure Q2(c)** using source transformation. (5 marks)
- (d) Use the nodal analysis to find the voltage at node 1, 2 and 3 in the circuit of **Figure Q2(d)**. (10 marks)

PART B:

- Q3** (a) Both the capacitor and inductor are passive elements. Explain the difference between a capacitor and an inductor. (4 marks)
- (b) Calculate the equivalent capacitance and inductance by simplifying the circuit in **Figure Q3(b)** to a single capacitor and a single inductor. (5 marks)
- (c) Determine V_c , i_L and the energy stored in the capacitor and inductor in the circuit shown in **Figure Q3(c)** under DC condition. (8 marks)
- (d) The switch in the circuit in **Figure Q3(d)** has been closed for a long time. It is opened at $t = 0$. Calculate the capacitor voltage $v(t)$ for $t > 0$. (8 marks)

- Q4** (a) Illustrate the following AC fundamental terms below using a voltage waveform as function of time.
- (i) Peak to peak value (2 marks)
 - (ii) Peak amplitude (2 marks)
- (b) Calculate the RMS value and the average value of the voltage wave shown in **Figure Q4(b)**. (5 marks)
- (c) As shown in **Figure Q4(c)**, a $150\ \Omega$ resistor (R), a $0.5\ \text{H}$ inductor (L) and a $100\ \mu\text{F}$ capacitor (C) are connected in series to a $50\ \text{Hz}$ source (V). The RMS current, I_{RMS} in the circuit is $10\ \text{A}$.
- (i) Determine the RMS voltage across the resistor, inductor and capacitor (6 marks)
 - (ii) Determine the RMS voltage across the RLC combination (4 marks)
 - (iii) Sketch the phasor diagram for this circuit (6 marks)

- Q5** (a) Sketch a basic transformer structure. Identify and label the core, primary winding and secondary winding. (4 marks)
- (b) An ideal transformer is rated at 2400/120V, 9.6kVa, and has 100 turns on the secondary side. Calculate:
- (i) The turn ratio (2 marks)
 - (ii) The number of turns on the primary side (2 marks)
 - (iii) The current rating for the primary and secondary winding (2 marks)
- (c) In digital system, different gates are connected to perform different functions. Such circuits are called combinational logic circuit. **Figure Q5(c)** shows a combinational logic circuit.
- (i) Obtain the complete Boolean expression for X (6 marks)
 - (ii) Using Boolean expression in **Q5(c)(i)**, derive a truth table for the function X. (6 marks)
 - (iii) Identify and draw the logic circuit for the simplified Boolean expression by using only a single logic gate that can be applied to replace the whole circuit. (3 marks)

-END OF QUESTIONS -

FINAL EXAMINATION

SEMESTER / SESSION : SEM II/ 2018/2019
 COURSE NAME: ELECTRICAL AND ELECTRONIC
 TECHNOLOGY

PROGRAMME CODE: BDD
 COURSE CODE: BDA 14303

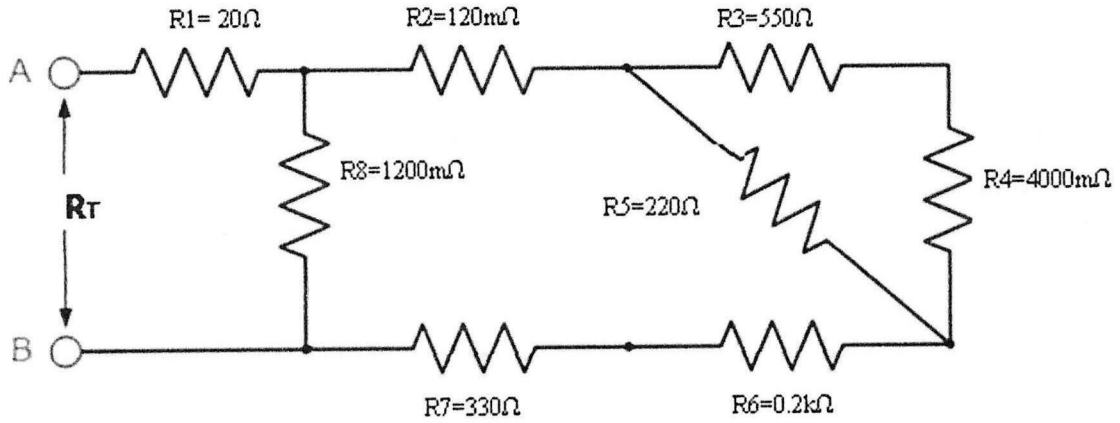


Figure Q1(c)

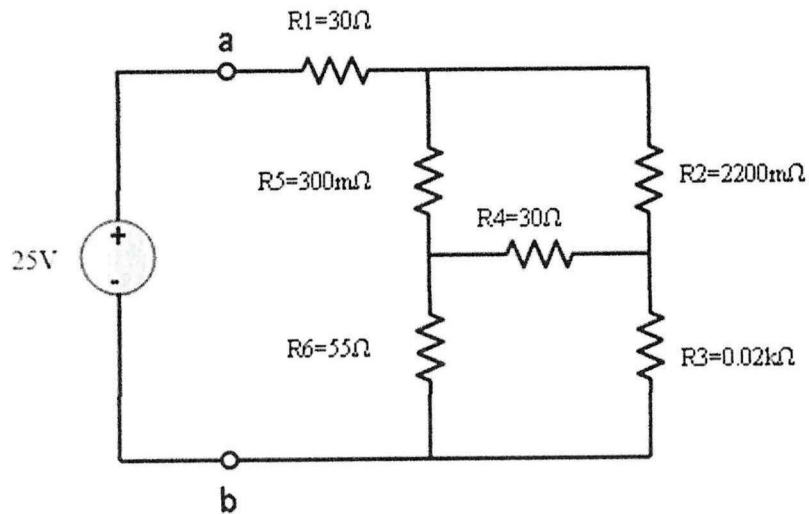


Figure Q1(d)

TERBUKA

FINAL EXAMINATION

SEMESTER / SESSION : SEM II / 2018/2019
 COURSE NAME: ELECTRICAL AND ELECTRONIC
 TECHNOLOGY

PROGRAMME CODE: BDD
 COURSE CODE: BDA 14303

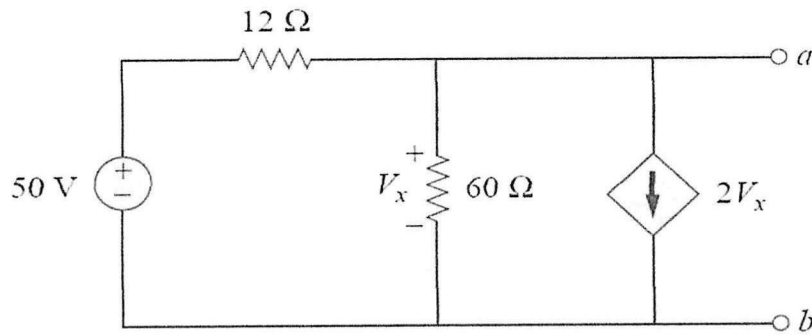


Figure Q2(b)

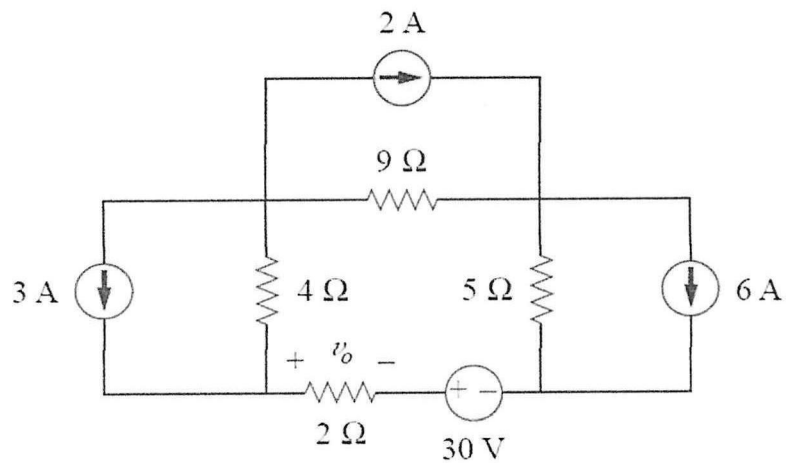


Figure Q2(c)

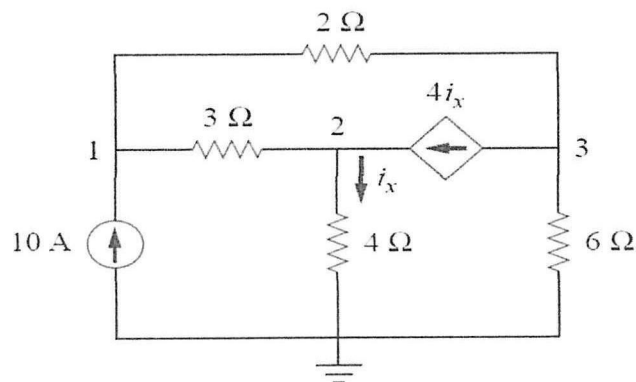


Figure Q2(d)

FINAL EXAMINATION

SEMESTER / SESSION : SEM II / 2018/2019
 COURSE NAME: ELECTRICAL AND ELECTRONIC
 TECHNOLOGY

PROGRAMME CODE: BDD
 COURSE CODE: BDA 14303

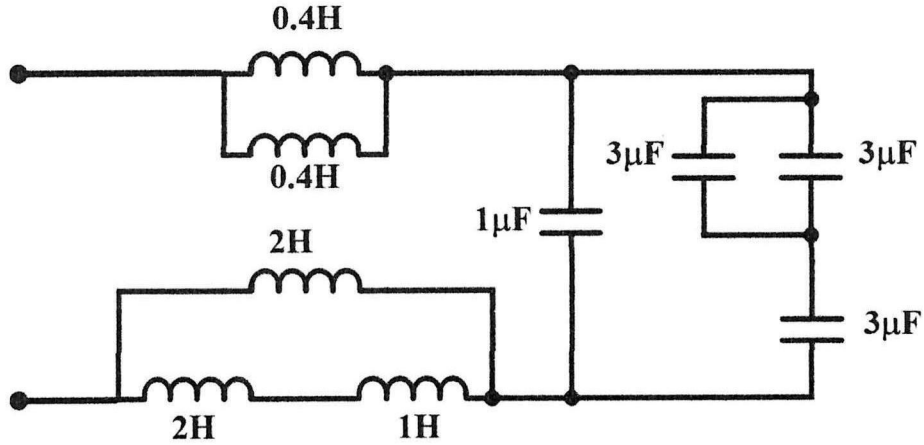


Figure Q3(b)

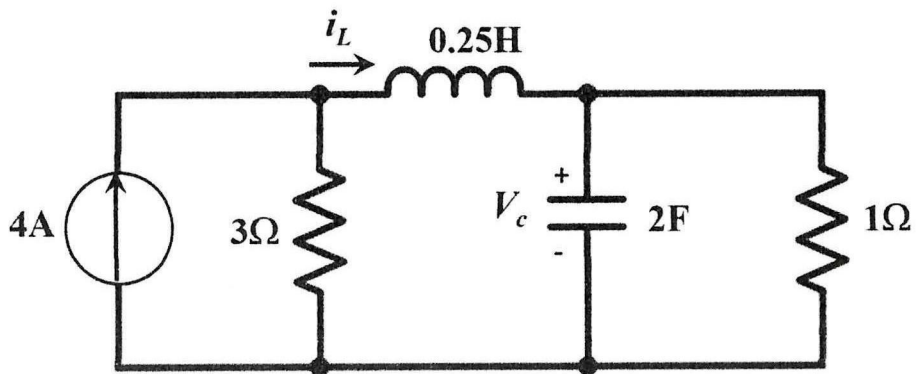


Figure Q3(c)

FINAL EXAMINATION

SEMESTER / SESSION : SEM II / 2018/2019
COURSE NAME: ELECTRICAL AND ELECTRONIC
TECHNOLOGY

PROGRAMME CODE: BDD
COURSE CODE: BDA 14303

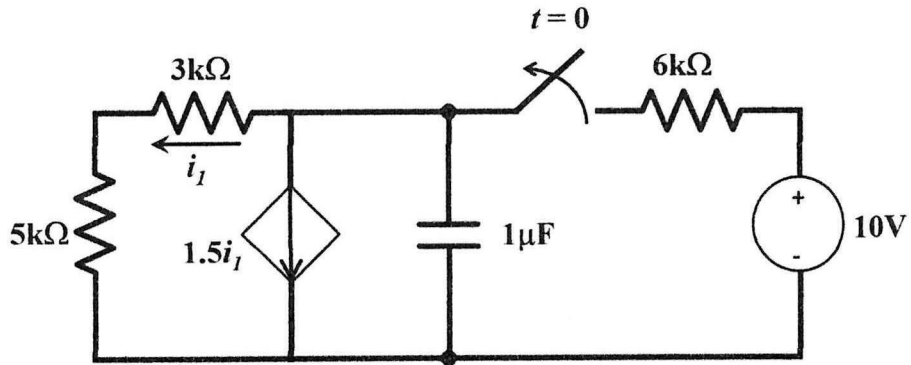


Figure Q3(d)

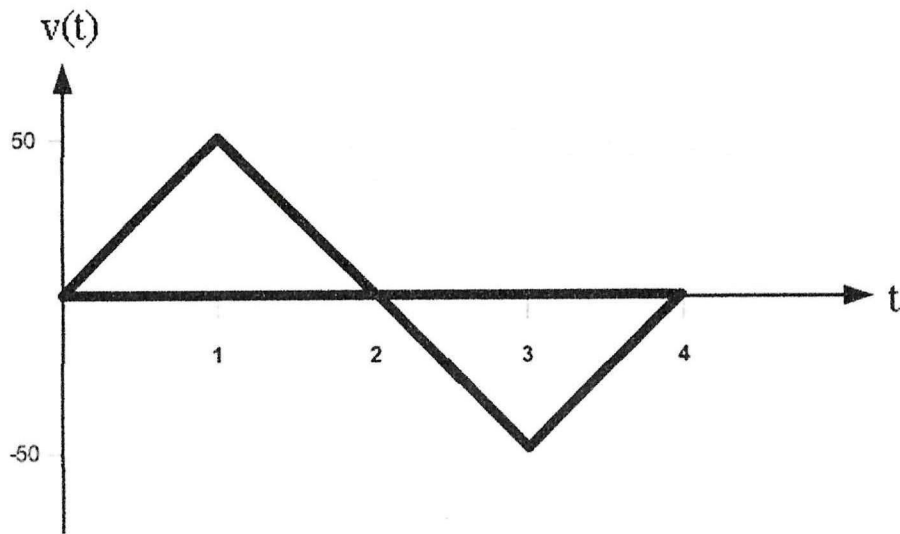


Figure Q4(b)

FINAL EXAMINATION

SEMESTER / SESSION : SEM II / 2018/2019
COURSE NAME: ELECTRICAL AND ELECTRONIC
TECHNOLOGY

PROGRAMME CODE: BDD
COURSE CODE: BDA 14303

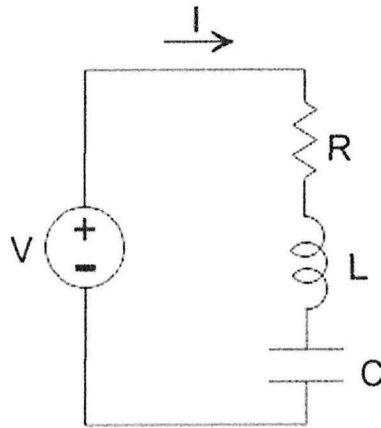


Figure Q4(c)

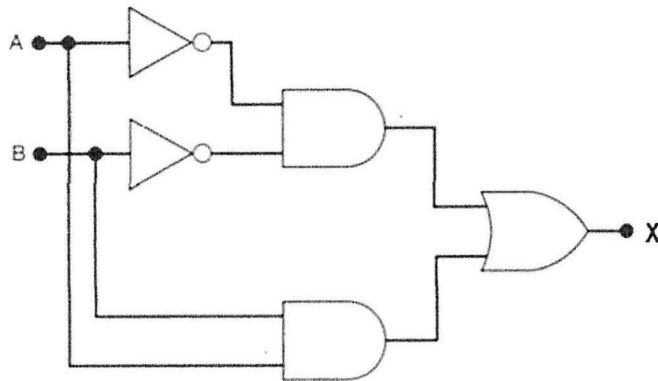


Figure Q5(c)

FINAL EXAMINATION

SEMESTER / SESSION : SEM II / 2018/2019
 COURSE NAME: ELECTRICAL AND ELECTRONIC TECHNOLOGY

PROGRAMME CODE: BDD
 COURSE CODE: BDA 14303

LIST OF FORMULA

OHMS LAW

$$V = IR$$

JOULE'S LAW

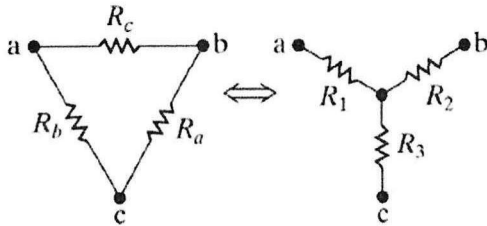
$$P = IV$$

KIRCHHOFF LAW

$$\sum_{k=1}^n i_k = 0$$

$$\sum_{v=1}^n v_k = 0$$

WYE-DELTA TRANSFORMATION



$$R_a = \frac{R_1 R_2 + R_2 R_3 + R_3 R_1}{R_1}$$

$$R_1 = \frac{R_b R_c}{R_a + R_b + R_c}$$

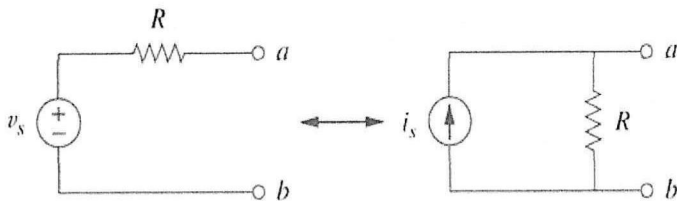
$$R_b = \frac{R_1 R_2 + R_2 R_3 + R_3 R_1}{R_2}$$

$$R_2 = \frac{R_c R_a}{R_a + R_b + R_c}$$

$$R_c = \frac{R_1 R_2 + R_2 R_3 + R_3 R_1}{R_3}$$

$$R_3 = \frac{R_a R_b}{R_a + R_b + R_c}$$

SOURCE TRANSFORMATION



$$V_s = I_s R$$

TERBUKA

FINAL EXAMINATION

SEMESTER / SESSION : SEM II / 2018/2019
 COURSE NAME: ELECTRICAL AND ELECTRONIC

PROGRAMME CODE: BDD
 COURSE CODE: BDA 14303

THEVENIN AND NORTON EQUIVALENT CIRCUIT

$$R_{TH} = R_N$$

$$I_N = \frac{V_{TH}}{R_{TH}}$$

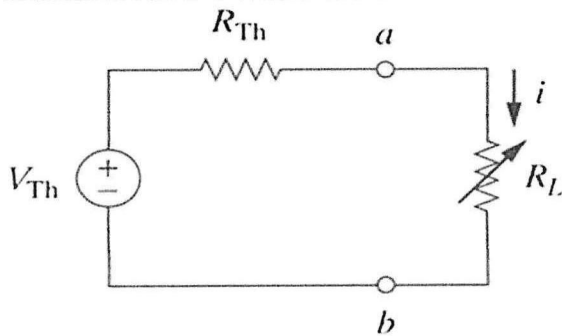
$$P = i^2 R_L = \left(\frac{V_{TH}}{R_{TH} + R_L} \right)^2 R_L$$

When $R_L \neq R_{TH}$

$$P_{max} = \frac{V_{TH}^2}{4R_{TH}}$$

When $R_L = R_{TH}$

MAXIMUM POWER TRANSFER



$$P = i^2 R_L = \left(\frac{V_{TH}}{R_{TH} + R_L} \right)^2 R_L$$

CAPACITOR AND INDUCTOR

$$C = \frac{\epsilon A}{d}$$

$$v(t) = \frac{1}{C} \int_{-\infty}^t i(t) dt + v(t_0)$$

$$i = C \frac{dv}{dt}$$

$$w = \frac{1}{2} C v^2$$

$$L = \frac{N^2 \mu A}{l}$$

$$v = L \frac{di}{dt}$$

$$i = \frac{1}{L} \int_{t_0}^t v(t) dt + i(t_0)$$

$$w = \frac{1}{2} L i^2$$

$$\tau = RC$$

$$\tau = \frac{L}{R}$$

FINAL EXAMINATION

SEMESTER / SESSION : SEM II / 2018/2019
 COURSE NAME: ELECTRICAL AND ELECTRONIC

PROGRAMME CODE: BDD
 COURSE CODE: BDA 14303

PHASOR REALTIONSHIP

$$v(t + T) = v(t)$$

$$f = \frac{1}{T}$$

$$z = x + jy = r \angle \phi = r(\cos \phi + j \sin \phi)$$

ALTERNATING CURRENT POWER CALCULATION

$$P(t) = v(t)i(t)$$

Instantaneous power

$$P = \frac{1}{2} \operatorname{Re}[VI^*] = \frac{1}{2} V_m I_m \cos(\theta_v - \theta_i)$$

Average power

$$i_{RMS} = \sqrt{\frac{1}{T} \int_0^T i^2 dt}$$

$$P_{RMS} = I_{RMS}^2 R = \frac{V_{RMS}^2}{R}$$

TRANSFORMERS

$$\frac{V_P}{V_S} = \frac{N_P}{N_S}$$

LOGIC GATES

Name	NOT	AND	NAND	OR	NOR	XOR	XNOR																																																																																																
Alg. Expr.	\bar{A}	AB	\overline{AB}	$A+B$	$\overline{A+B}$	$A \oplus B$	$\overline{A \oplus B}$																																																																																																
Symbol																																																																																																							
Truth Table	<table border="1"> <tr><th>A</th><th>X</th></tr> <tr><td>0</td><td>1</td></tr> <tr><td>1</td><td>0</td></tr> </table>	A	X	0	1	1	0	<table border="1"> <tr><th>B</th><th>A</th><th>X</th></tr> <tr><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>1</td></tr> </table>	B	A	X	0	0	0	0	1	0	1	0	0	1	1	1	<table border="1"> <tr><th>B</th><th>A</th><th>X</th></tr> <tr><td>0</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>0</td></tr> </table>	B	A	X	0	0	1	0	1	1	1	0	1	1	1	0	<table border="1"> <tr><th>B</th><th>A</th><th>X</th></tr> <tr><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>1</td></tr> </table>	B	A	X	0	0	0	0	1	1	1	0	1	1	1	1	<table border="1"> <tr><th>B</th><th>A</th><th>X</th></tr> <tr><td>0</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>0</td></tr> </table>	B	A	X	0	0	1	0	1	0	1	0	0	1	1	0	<table border="1"> <tr><th>B</th><th>A</th><th>X</th></tr> <tr><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>0</td></tr> </table>	B	A	X	0	0	0	0	1	1	1	0	1	1	1	0	<table border="1"> <tr><th>B</th><th>A</th><th>X</th></tr> <tr><td>0</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>1</td></tr> </table>	B	A	X	0	0	1	0	1	0	1	0	0	1	1	1
A	X																																																																																																						
0	1																																																																																																						
1	0																																																																																																						
B	A	X																																																																																																					
0	0	0																																																																																																					
0	1	0																																																																																																					
1	0	0																																																																																																					
1	1	1																																																																																																					
B	A	X																																																																																																					
0	0	1																																																																																																					
0	1	1																																																																																																					
1	0	1																																																																																																					
1	1	0																																																																																																					
B	A	X																																																																																																					
0	0	0																																																																																																					
0	1	1																																																																																																					
1	0	1																																																																																																					
1	1	1																																																																																																					
B	A	X																																																																																																					
0	0	1																																																																																																					
0	1	0																																																																																																					
1	0	0																																																																																																					
1	1	0																																																																																																					
B	A	X																																																																																																					
0	0	0																																																																																																					
0	1	1																																																																																																					
1	0	1																																																																																																					
1	1	0																																																																																																					
B	A	X																																																																																																					
0	0	1																																																																																																					
0	1	0																																																																																																					
1	0	0																																																																																																					
1	1	1																																																																																																					