UTHM
Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2018/2019

COURSE NAME	:	ELECTRICAL AND ELECTRONIC TECHNOLOGY
COURSE CODE	:	BDA 14303
PROGRAMME CODE	:	BDD
EXAMINATION DATE	:	DECEMBER 2018/ JANUARY 2019
DURATION	:	3 HOURS
INSTRUCTION	:	ANSWER **FOUR (4)** QUESTIONS ONLY

THIS QUESTION PAPER CONSISTS OF **TWELVE (12)** PAGES

Q1 (a) Explain the definition of terms below in electricity.

(i) Voltage
(ii) Current

(2 marks)

(b) Give two (2) examples of DC voltage sources.

(2 marks)

(c) The voltage across an electric element is 4V. The energy used by the element is 30 Joules within 5 minutes. Determine the current, I flow through the element.

(4 marks)

(d) As shown in **Figure Q1(d)**, calculate the currents I_1 and I_2 that flow in the circuit.

(5 marks)

(e) Referring to **Figure Q1(e)**, use the Wye-Delta Transformation to determine the total resistance, R_T and the voltage Vo. Given the source current, I is 5 mA.

(12marks)

Q2 (a) (i) Explain the steps required to obtain the solution in electric circuits by mesh analysis.

(4 marks)

(ii) As shown in **Figure Q2(a),** use mesh analysis to find the current i_o. Given at node A; $i_1 = i_2 + i_o$.

(8 marks)

(b) As shown in **Figure Q2(b)**, a 120Ω resistor (R1), a 360Ω resistor (R2) and a 240Ω resistor (R3) are connected to a 28V voltage source (Vs1) and a 12V voltage source (Vs2). Using nodal analysis, determine the current flows in R2 and the power consumption of R3.

(6 marks)

(c) As shown in **Figure Q2(c),** a 3Ω resistor (R1), a 6Ω resistor (R2) and a 5Ω resistor (R3) are connected to a 10V voltage source (V_{S1}). Using Thevenin's Theorem calculate the value of Vth and the Rth of the circuit.

(7 marks)

Q3 (a) With simple sketches, illustrate how circuits with energy storage elements behave differently than circuits without energy storage elements.

(4 marks)

(b) Determine the equivalent capacitance and inductance by simplify the circuit in **Figure Q3(b)** to a single inductor and a single capacitor.

(6 marks)

(c) You need a 3 pF capacitor, but the electronics component store only has 1.8 pF, 4.7 pF and 5.6 pF capacitors. The owner proposed to you a configuration of these capacitors as shown in **Figure Q3(c).** Will this combination give you the desired value?

(5 marks)

(d) The switch in the circuit in **Figure Q3(d)** has been closed for a long time. It is opened at $t = 0$. Calculate the capacitor voltage $v(t)$ for $t > 0$.

(10 marks)

Q4 (a) Sketch the sin waveform and the cosine waveform for ac voltage and ac current.

(4 marks)

(b) An AC circuits with 60 Hz voltage of 240V effective value is impressed on an inductance of 0.256 H.

(i) Write the time equation for the voltage and the resulting current. Let the zero axis of the voltage wave be at t=0.

(3 marks)

(ii) Sketch the phasor diagram for this circuit

(3 marks)

(iii) Find the maximum energy stored in the inductance.

(3 marks)

(c) Consider the circuit as shown in **Figure Q4(c)** with $v(t) = 3 + 6t^2 + 2\sin 8t \ V$.

(i) At t=0, what will the current $i_R(0)$ in the resistor be?

(2 marks)

(ii) Write the current equation of $i_R(t)$

(2 marks)

(iii) Determine the current equation of $i_C(t)$

(3 marks)

(iv) With the assumption of $i_L(0) = 9A$, determine the value of $i(t)$ at t=0. Write the current equation of $i_L(t)$.

(3 marks)

(v) Determine the current equation of $i(t)$.

(2 marks)

Q5 (a) (i) With simple sketches, illustrate the working principles of DC motor.

(5 marks)

(ii) State three (3) differences between AC and DC motor.

(3 marks)

(b) (i) Construct a truth table for the logical functions at the points P, Q and R in the logic diagram of **Figure Q5(b)(i)**. Identify a single logic get that can be applied to replace the whole circuit.

(5 marks)

(ii) Derive the Boolean expression for the logic circuit shown in **Figure Q5(b)(ii)**.

(6 marks)

(iii) Construct the logic circuit based on the Boolean expression.

$$Q = (A \cdot B \cdot C) + A \cdot \left(\overline{B} + \overline{C}\right)$$

(6 marks)

-END OF QUESTIONS –

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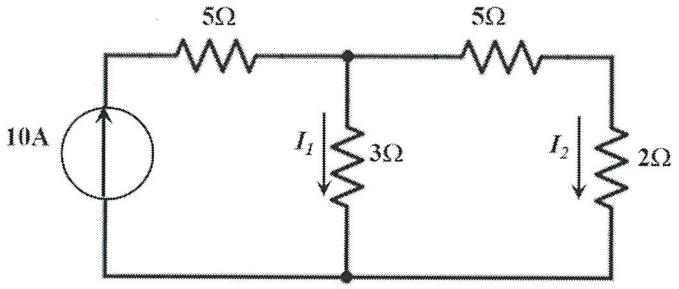

Figure Q1(d)

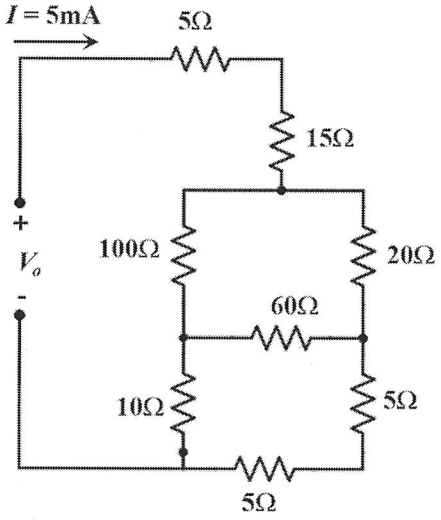

Figure Q1(e)

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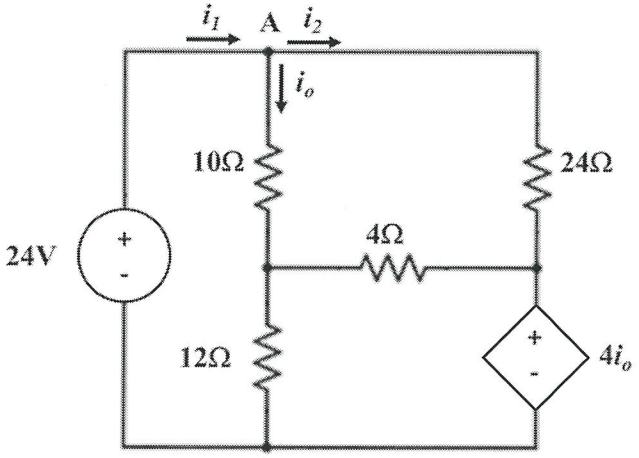

Figure Q2(a)

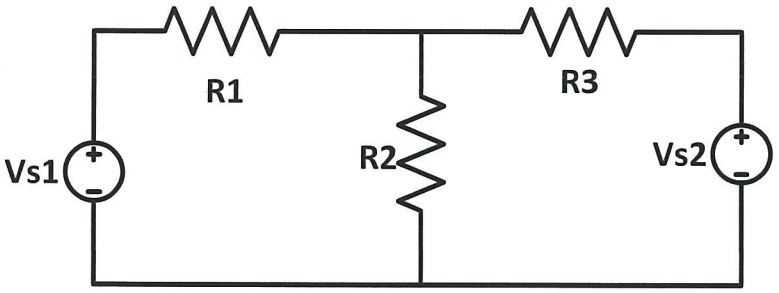

Figure Q2(b)

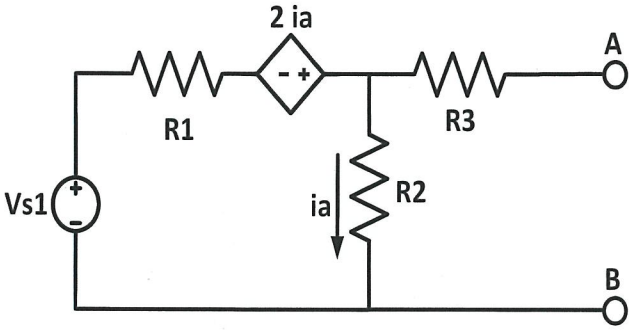

Figure Q2(c)

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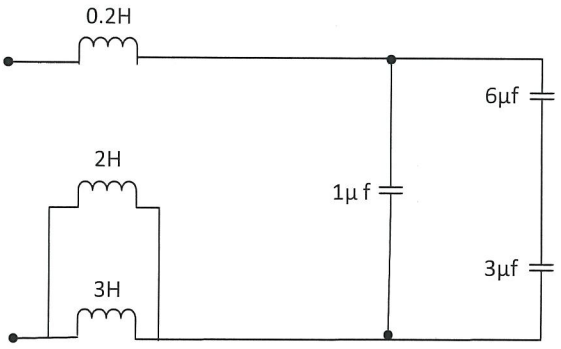

Figure Q3(b)

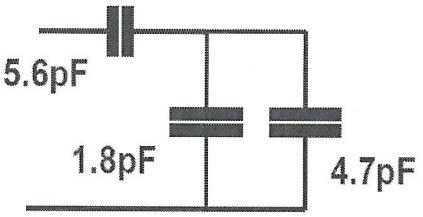

Figure Q3(c)

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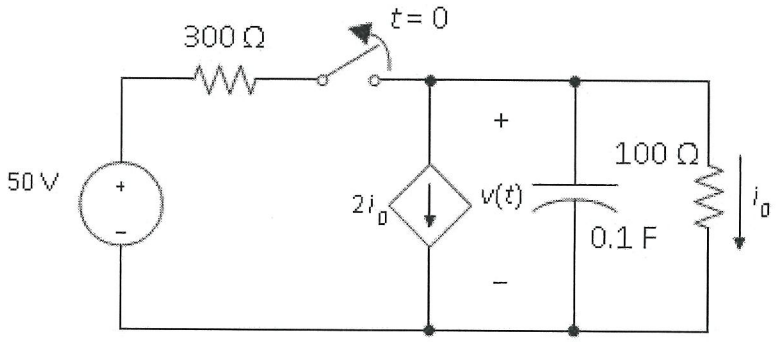

Figure Q3(d)

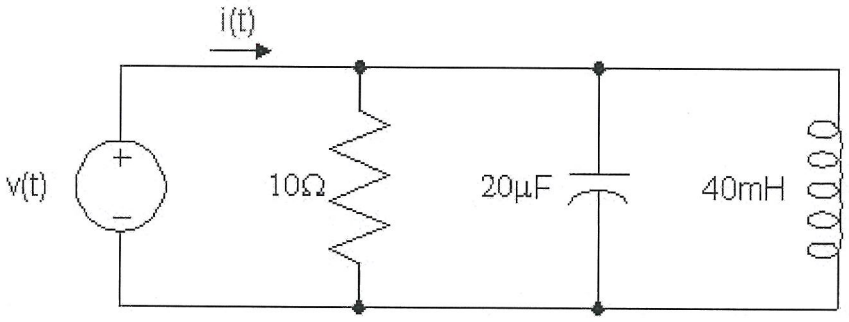

Figure Q4(c)

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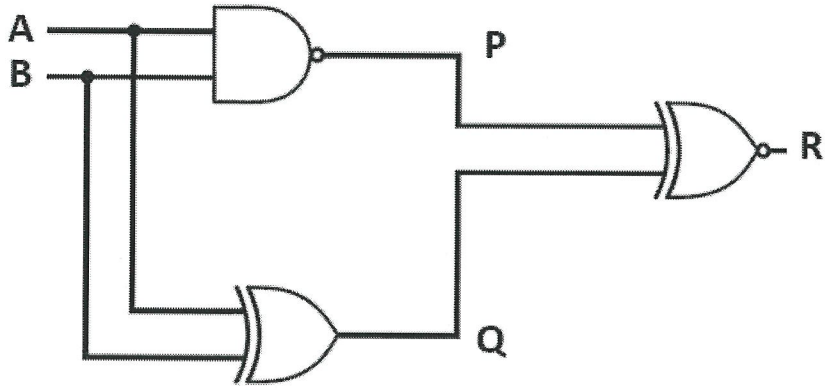

Figure Q5(b)(i)

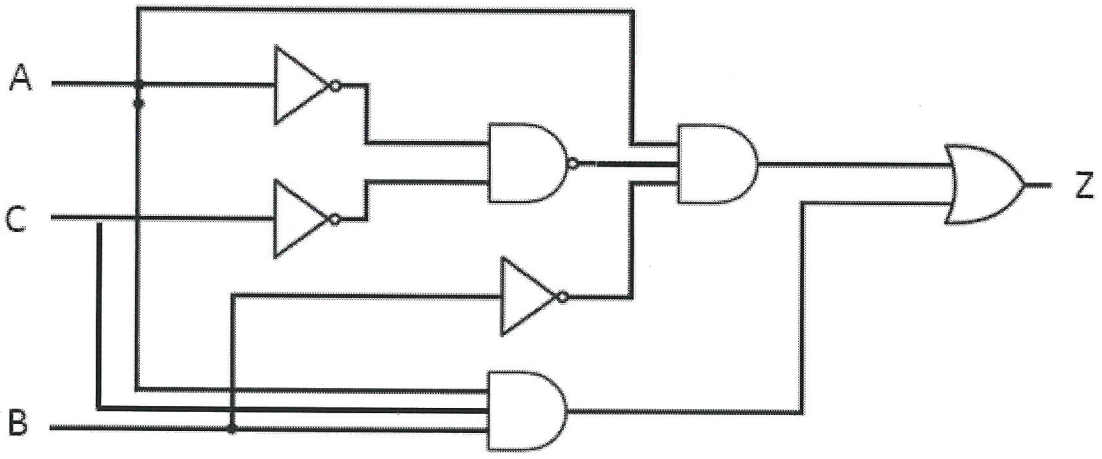

Figure Q5(b)(ii)

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LIST OF FORMULA

OHMS LAW

$$V = IR$$

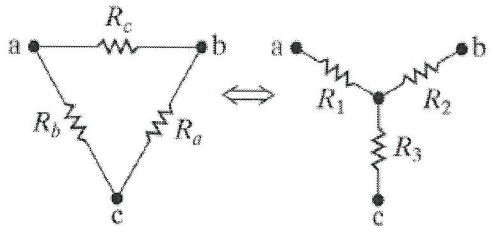
JOULE'S LAW

$$P = IV$$

KIRCHHOFF LAW

$$\sum_{k=1}^{n} i_k = 0 \qquad \sum_{v=1}^{n} v_k = 0$$

WYE-DELTA TRANSFORMATION

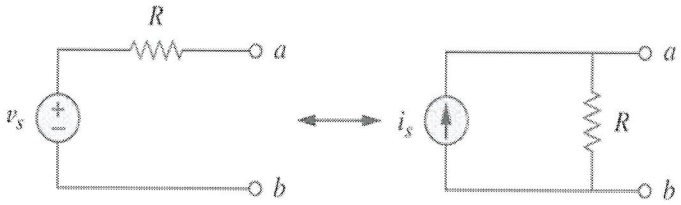


$$R_a = \frac{R_1R_2 + R_2R_3 + R_3R_1}{R_1} \qquad R_1 = \frac{R_bR_c}{R_a + R_b + R_c}$$

$$R_b = \frac{R_1R_2 + R_2R_3 + R_3R_1}{R_2} \qquad R_2 = \frac{R_cR_a}{R_a + R_b + R_c}$$

$$R_c = \frac{R_1R_2 + R_2R_3 + R_3R_1}{R_3} \qquad R_1 = \frac{R_aR_b}{R_a + R_b + R_c}$$

SOURCE TRANSFORMATION



$$V_S = I_sR$$

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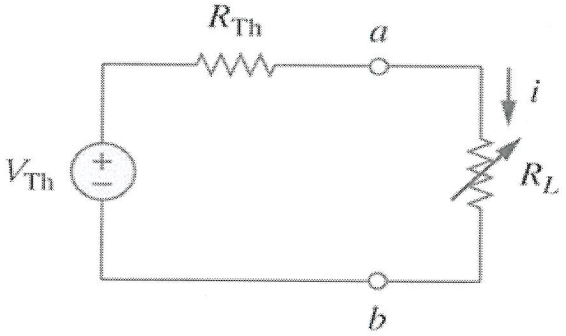
THEVENIN AND NORTON EQUIVALENT CIRCUIT

$$R_{TH} = R_N \qquad I_N = \frac{V_{TH}}{R_{TH}}$$

$$P = i^2 R_L = \left(\frac{V_{TH}}{R_{TH} + R_L} \right)^2 R_L \qquad \text{When } R_L \neq R_{TH}$$

$$P_{max} = \frac{V_{TH}^{\ 2}}{4R_{TH}} \qquad \text{When } R_L = R_{TH}$$

MAXIMUM POWER TRANSFER



$$P = i^2 R_L = \left(\frac{V_{TH}}{R_{TH} + R_L} \right)^2 R_L$$

CAPACITOR AND INDUCTOR

$$C = \frac{\varepsilon A}{d} \qquad v(t) = \frac{1}{C}\int_{-\infty}^{t} i(t)dt + v(t_0)$$

$$i = C\frac{dv}{dt} \qquad w = \frac{1}{2}Cv^2$$

$$L = \frac{N^2 \mu A}{l} \qquad v = L\frac{di}{dt}$$

$$i = \frac{1}{L}\int_{t_0}^{t} v(t)dt + i(t_0) \qquad w = \frac{1}{2}Li^2$$

$$\tau = RC \qquad \tau = \frac{L}{R}$$

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PHASOR REALTIONSHIP

$$v(t+T)=v(t)$$

$$f=\frac{1}{T}$$

$$z=x+jy=r\angle\phi=r(\cos\phi+j\sin\phi)$$

ALTERNATING CURRENT POWER CALCULATION

$$P(t)=v(t)i(t)$$ Instantaneous power

$$P=\frac{1}{2}\mathrm{Re}[VI^*]=\frac{1}{2}V_m I_m\cos(\theta_v-\theta_i)$$ Average power

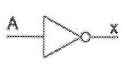
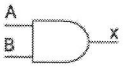
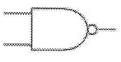
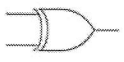
$$i_{RMS}=\sqrt{\frac{1}{T}\int_0^T i^2dt}$$

$$P_{RMS}=I_{RMS}{}^2R=\frac{V_{RMS}{}^2}{R}$$

TRANSFORMERS

$$\frac{V_P}{V_S}=\frac{N_P}{N_S}$$

LOGIC GATES

Name	NOT	AND	NAND	OR	NOR	XOR	XNOR
Alg. Expr.	$\overline{A}$	AB	$\overline{AB}$	$A+B$	$\overline{A+B}$	$A\oplus B$	$\overline{A\oplus B}$
Symbol							

Truth Table

A	X
0	1
1	0

B	A	X
0	0	0
0	1	0
1	0	0
1	1	1

B	A	X
0	0	1
0	1	1
1	0	1
1	1	0

B	A	X
0	0	0
0	1	1
1	0	1
1	1	1

B	A	X
0	0	1
0	1	0
1	0	0
1	1	0

B	A	X
0	0	0
0	1	1
1	0	1
1	1	0

B	A	X
0	0	1
0	1	0
1	0	0
1	1	1