UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2012/2013

COURSE NAME	:	LOGIC SYSTEMS
COURSE CODE	:	DAE 21603
PROGRAMME	:	2 DAE
EXAMINATION DATE	:	OCTOBER 2012
DURATION	:	2½ HOURS
INSTRUCTIONS	:	ANSWER **FOUR (4)** QUESTIONS ONLY

THIS QUESTION PAPER CONSISTS OF NINE (9) PAGES

Q1 (a) Give the truth table of the RS flip-flop. Realize the RS flip-flop using:

(i) NAND Gates only
(ii) NOR Gates only.

(6 marks)

(b) A D flip-flop is sometimes used to delay a binary waveform. A D flip-flop with timing diagram for input data and clock input are as shown in Figure Q1(b).

(i) Draw the Q output waveform on the space provided.
(ii) By referring to the timing diagram, explain the operation of the D flip-flop.

(6 marks)

(c) Figure Q1(c) shows a 7476 JK flip-flop and timing diagram showing the clock input and two asynchronous inputs. By considering the input for both J and K are always HIGH and Q is initially LOW:

(i) Draw the Q output waveform.
(ii) Explain the operation of this JK flip-flop.

(9 marks)

(d) Show how to create the following flip flops from JK flip flop:

(i) D flip flop
(ii) T flip flop

(4 marks)

Q2 (a) What are the essential differences between synchronous and asynchronous counters.

(4 marks)

(b) (i) Construct a 4 bit ripple counter and explain its operation with the help of timing diagrams
(ii) Convert the 4 bit ripple counter to a MOD 9 counter.

(10 marks)

(c) Explain the operation of the up/down counter shown in Figure Q2(c) by analysing the inputs to the clock of the flip-flop. Sketch logic and timing diagrams for both up and down sequence.

(11 marks)

Q3 (a) Determine the number of flip-flops needed to construct a shift register capable of storing:

(i) a 6-bit binary number
(ii) decimal numbers up to 32
(iii) hexadecimal numbers up to F.

(5 marks)

(b) Figure Q3(b) shows a 4-bit serial input register and timing diagrams showing the clock and data inputs. Draw the output waveforms for four clock transitions.

(8 marks)

(c) With the aid of logic circuits and tables showing the sequence of states, describe the differences between a Ring counter and a Johnson counter.

(12 marks)

Q4 (a) What are the basic **five** (5) steps taken to create and load a digital circuit into a PLD?

(5 marks)

(b) Name **three** (3) advantages of constructing a digital circuit prototype using a PLD instead of standard logic devices.

(3 marks)

(c) Several types of architecture are used in PLDs. Draw the block diagram of three common types and describe their differences.

(6 marks)

(d) For the functions shown on the K-maps in Figure Q4(d):
(i) Minimize the functions X, Y, Z and write down the minimized expressions.
(ii) Implement them on the PAL shown in Figure Q4(d)(ii). Label the inputs and outputs.

(11 marks)

Q5 (a) Figure Q5(a) shows a simplified view of a typical computer system.

(i) Name the semiconductor memory devices used.
(ii) Explain the differences between the three storage devices.

(8 marks)

(b) Compare the characteristics of RAM, ROM and EPROM.

(6 marks)

(c) List and explain two types of RAM.

(5 marks)

(d) List and describe the three major operations in a flash memory.

(6 marks)

Q6 (a) Show the following connections:

(i) Use JK flip-flops to divide a digital signal frequency by 8.
(ii) Use D-type flip-flops to divide a digital signal frequency by 4.

(8 marks)

(b) The logic diagram and Dual-In-Line Package for IC 7493 is given in Figure Q6(b). Do the following and show all steps.

(i) Name the three standard MOD counters that can be implemented.
(ii) Design a 7493-based Mod-13 counter. If the input clock frequency is 2 kHz, what is the output frequency of this counter?

(11 marks)

(c) Determine the maximum input clock frequency (f_{max}) for the counter shown in Figure Q6(c) if the propagation delay, t_{pd} for each flip-flop is 50 ns and t_{pd} for AND gate is 20 ns. Compare this with a MOD-16 ripple counter.

(6 marks)

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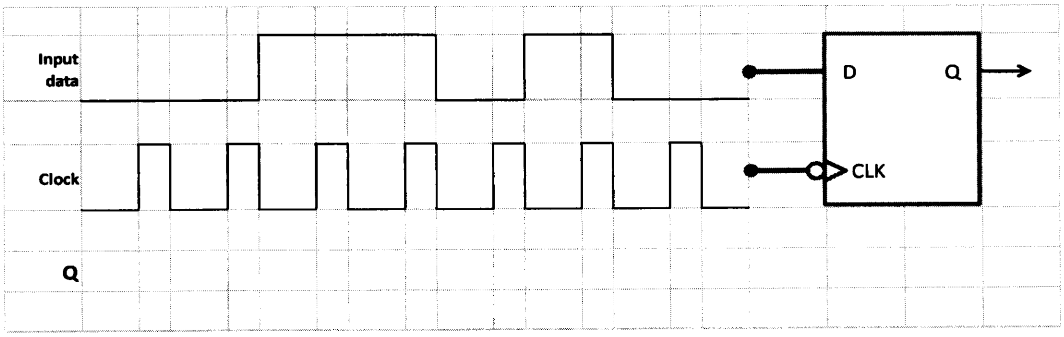

Figure Q1(b)

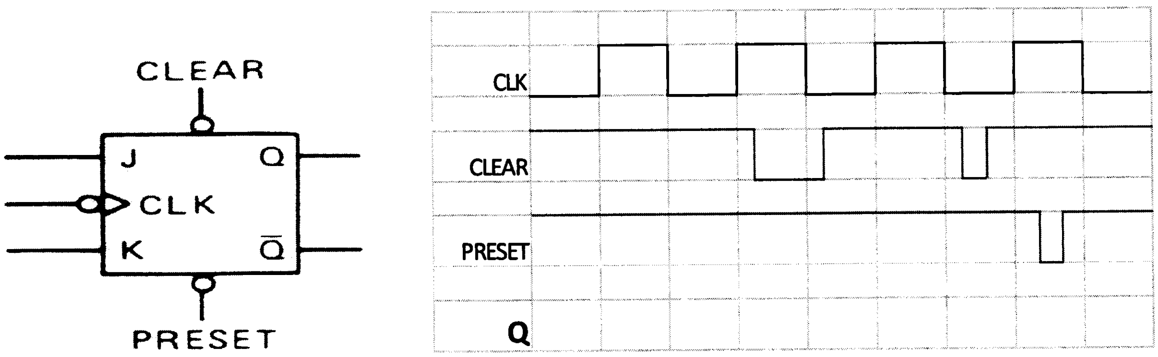

Figure Q1(c)

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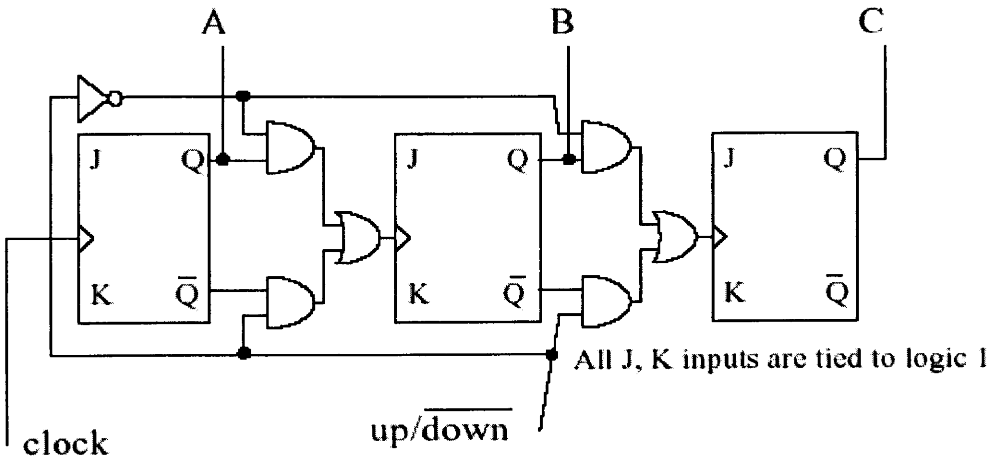

Figure Q2(c)

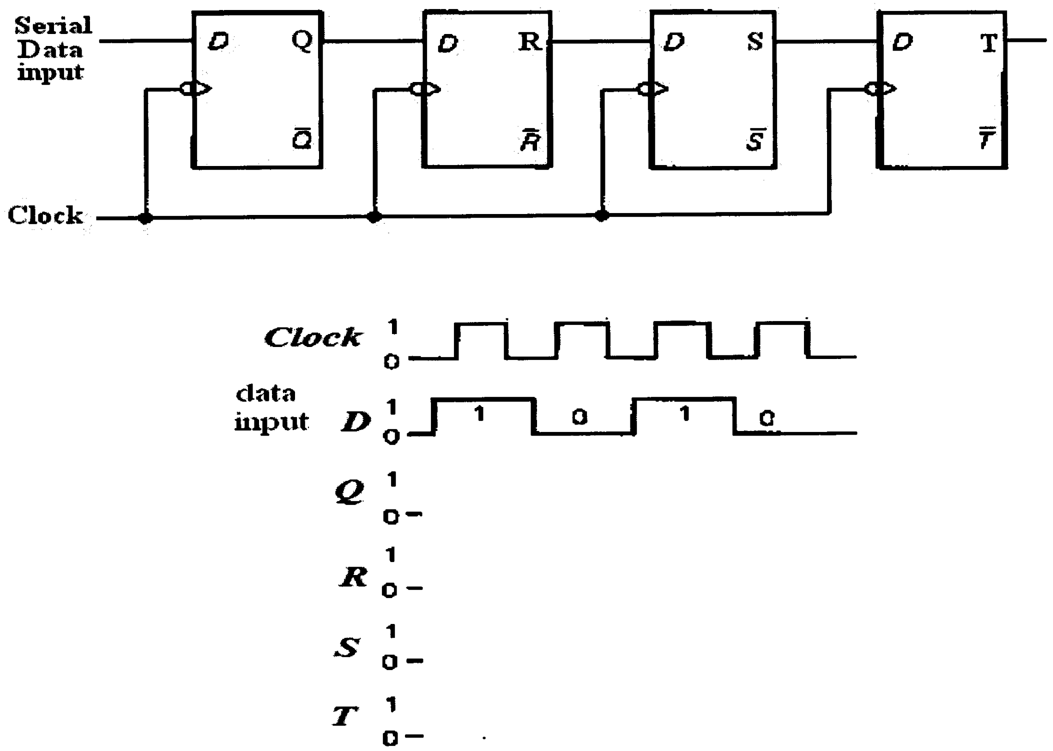

Figure Q3(b)

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X

CD \ AB	00	01	11	10
00				1
01	1	1		1
11	1	1		1
10				

Y

CD \ AB	00	01	11	10
00	1	1	1	1
01		1		
11		1		1
10	1			1

Z

CD \ AB	00	01	11	10
00			1	
01	1	1	1	
11	1	1	1	
10	1		1	1

Figure Q4(d)

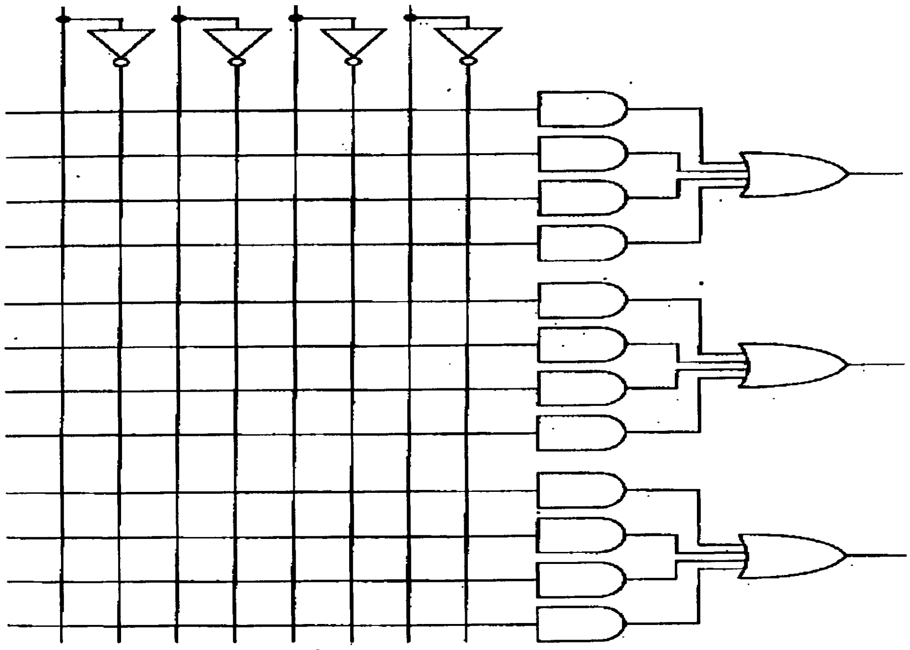

Figure Q4(d)(ii)

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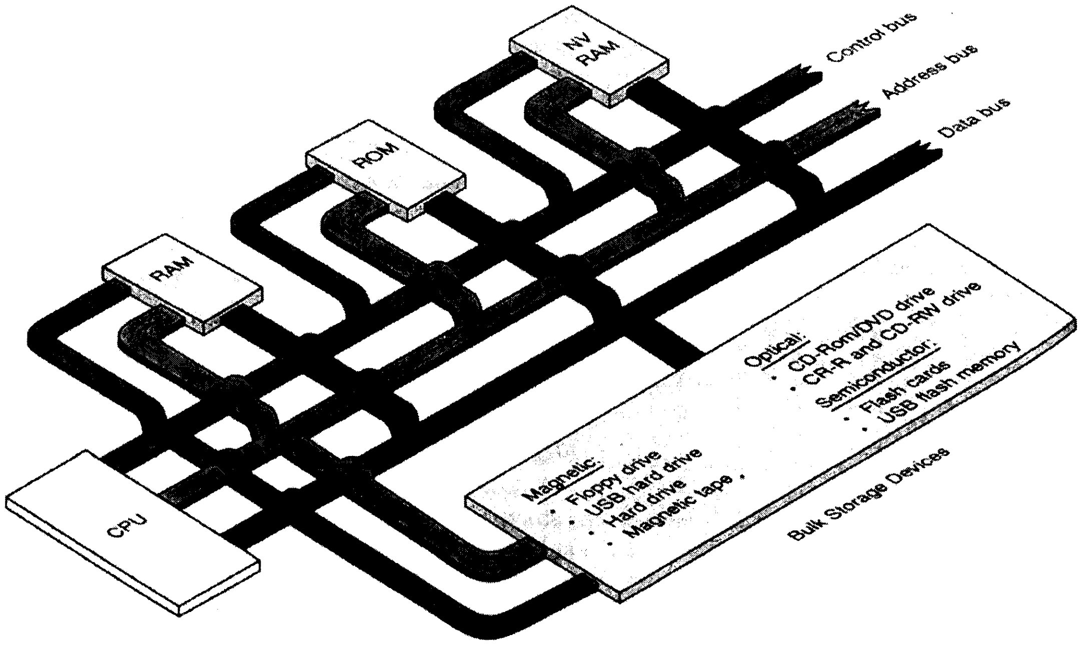

Figure Q5(a)

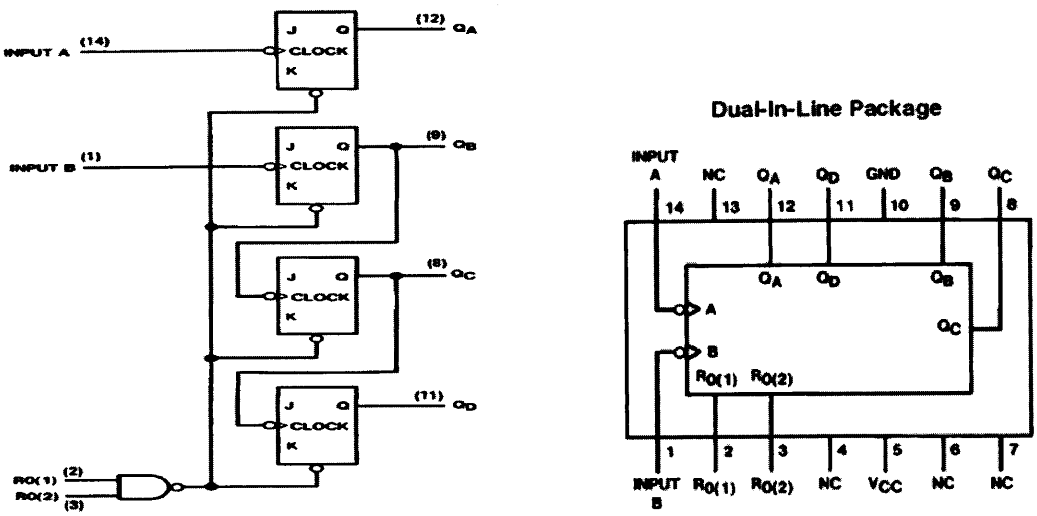

Figure Q6(b)

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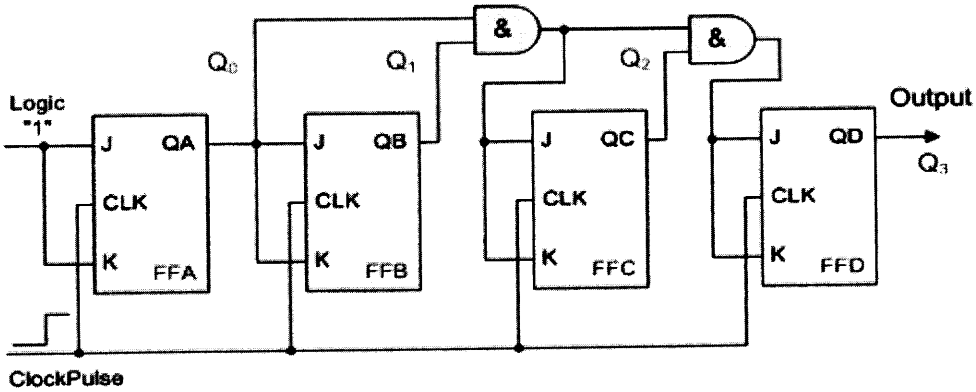

Figure Q6(c)