Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2019/2020

COURSE NAME	:	ELECTRONICS CIRCUITS AND DEVICES/ ELECTRONICS PRINCIPLE/ ELECTRONICS PRINCIPLE I
COURSE CODE	:	BNR 25803/ BNR 20503/ BNR 27103
PROGRAMME CODE	:	BND / BNE / BNF
EXAMINATION DATE	:	DECEMBER 2019/ JANUARY 2020
DURATION	:	3 HOURS
INSTRUCTION	:	ANSWER **ALL** QUESTIONS

THIS QUESTION PAPER CONSISTS OF **FIVE (5)** PAGES

Q1 (a) Define extrinsic semiconductors.

(2 marks)

(b) Distinguish **TWO (2)** differences between n-type and p-type semiconductors.

(4 marks)

(c) Draw relevant energy level diagrams of n-type and p-type semiconductors.

(4 marks)

(d) Explain **TWO (2)** reasons a pure semiconductor behaves like an insulator at absolute zero temperature.

(4 marks)

(e) Photodiode is usually operated under reverse biased condition.

(i) Define reverse biased condition

(2 marks)

(ii) Sketch voltage-current graph for the reverse biased p-n junction

(3 marks)

(f) With the help of a circuit diagram, explain how to use zener diode as a voltage regulator.

(6 marks)

Q2 (a) Sketch current-voltage (IV) characteristic of forward-biased and reverse-biased p-n junction practical diode.

(7 marks)

(b) Calculate the current for the circuit in **Figure Q2 (b)**.

(8 marks)

(c) Illustrate and completely label the output waveform for the circuits as shown **in Figure Q2 (c)**. Assume all the diodes are Silicon with clipping applications. Show all steps in obtaining the waveforms.

(10 marks)

Q3 (a) Design a voltage divider bias circuit in **Figure Q3 (a)** having $I_{BQ} = 60\mu A$, $V_E=0.1Vcc$ and $I_{Csat} = 8mA$ with R1 = 47kΩ and R2 =4.7kΩ. The supply voltage is 20V. Assume $\beta_{RE} \geq 10R_2$.

(b) Sketch the DC load line and determine the Q-points, I_{CQ} and V_{CEQ}.

(c) If β is changed two times than previous, construct the new Q-point and calculate the % of changes in the Ic and V_{CE}

(25 marks)

Q4 (a) List the comparison between BJT and MOSFET.

(10 marks)

(b) Consider NMOS circuit in **Figure Q4 (b)** with K = 0:25 mA/V^2 and V_t = 2 V. Find Vo when V_i = 0, 6, and 12 V for R_D = 1 K and V_{DD} = 12 V. Find the status circuit of each Vi.

(15 marks)

- END OF QUESTIONS -

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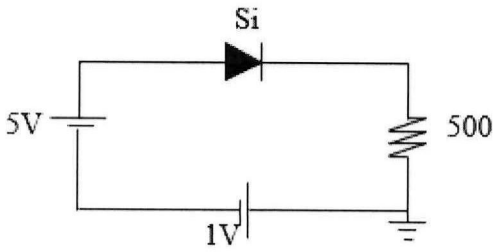

Figure Q2 (b)

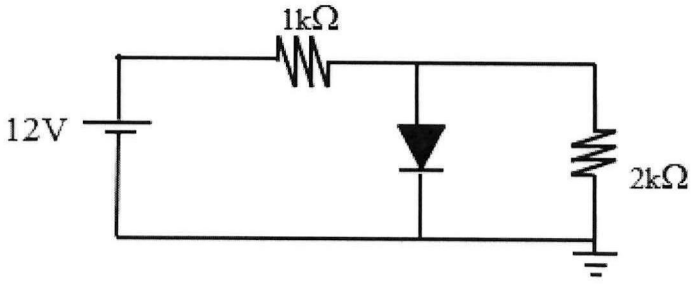

Figure Q2 (c)

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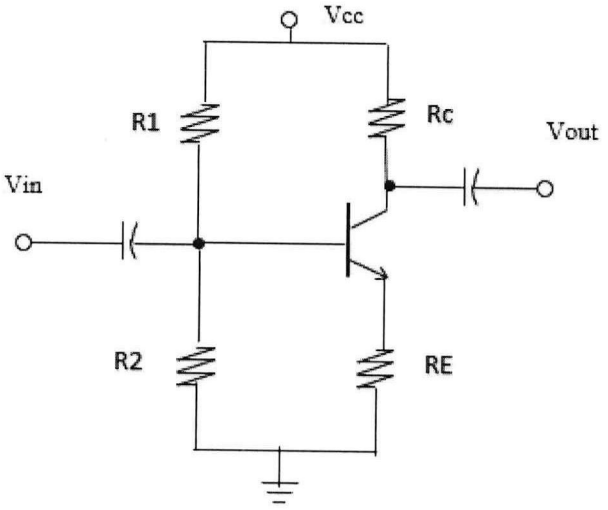

Figure Q3 (a)

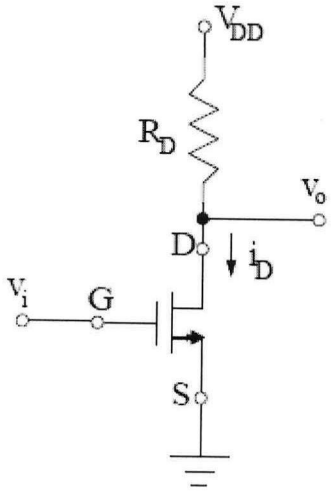

Figure Q4 (b)