Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2019/2020

COURSE NAME	:	ELECTRONIC DIGIT
COURSE CODE	:	BNR 25402
PROGRAMME CODE	:	BND
EXAMINATION DATE	:	DECEMBER 2019 / JANUARY 2020
DURATION	:	2 HOURS
INSTRUCTION	:	1. ANSWER **ALL** QUESTIONS 2. ATTACH **APPENDIX A** WITH YOUR ANSWER BOOKLET

THIS QUESTION PAPER CONSISTS OF **NINE (9)** PAGES

Q1 (a) Describe the main advantage of parallel transfer over serial transfer of binary data.

(2 marks)

(b) Perform the following operation:

(i) $10001100_2 + 00111001_2$

(ii) $C8_{16} - 3B_{16}$

(iii) BCD number: 10011000 + 10010111

(9 marks)

(c) Using Boolean Algebra, prove that:

$$\overline{A}\,\overline{B}C + \overline{(A + B + C)} + \overline{A}\,\overline{B}\,\overline{C}D = \overline{A}\,\overline{B}C + \overline{A}\,\overline{B}D$$

Given rules of Boolean Algebra:

$(A + 0 = A,\ A + 1 = 1,\ A + A = A,\ A + \overline{A} = 1,\ A + \overline{A}B = A + B)$

(4 marks)

(d) **Figure Q1(d)** shows a combinational logic circuit. From the **Figure Q1(d)**:

(i) write the Boolean expression for output X and simplify it using De Morgan Theorem.

(5 marks)

(ii) determine the value of output X for all possible input conditions and list the values in a truth table.

(5 marks)

Q2 (a) Explain the difference between sum-of-product (SOP) and product-of-sum (POS) expressions.

(2 marks)

(b) Use Karnaugh map to simplify the following expression to minimum POS form:

$$F = (X + Y)(W + Z)(X + Y + \overline{Z})(W + X + Y + Z)$$

(6 marks)

(c) **Figure Q2(c)** shows the inputs and output patterns of a logic circuit. The inputs are WXY and the output is Z.

(i) Obtain the truth table for this circuit.

(5 marks)

(ii) Write the output expression in SOP form.

(4 marks)

(iii) Simplify the output expression using Karnaugh map and implement this circuit using NAND gates ONLY.

(8 marks)

Q3 (a) (i) Briefly explain what is meant by a decoder.

(2 marks)

(ii) State the difference between a decoder and an encoder.

(2 marks)

(b) **Table Q3(b)** shows the truth table of a combinational logic circuit.

(i) Draw the gate using ONLY a 4:1 multiplexer and an inverter.

(7 marks)

(ii) Draw the gate using ONLY one 74x151 8:1 multiplexer chip with input/output as shown in **Figure Q3(b)**.

(8 marks)

(c) Use the 74138 IC as depicted in **Figure Q3(c)** to implement the following function.

$$W = A\overline{B}\,\overline{C} + C + AB$$

$$Y = AC + AB + \overline{A}B\overline{C} + \overline{A}\,\overline{C}$$

(6 marks)

Q4 (a) State the differences between latch and flip-flop. List **THREE (3)** types of latches and flip-flop.

(4 marks)

(b) With the aid of truth tables, describe the differences among the following flip-flops.

(i) RS flip-flop

(2 marks)

(ii) JK flip-flop

(2 marks)

(iii) D flip-flop

(2 marks)

(c) Sketch the gate-level circuit for a NOR-based SR latch.

(3 marks)

(d) **Figure Q4(d)(i)** shows a logic circuit that comprises of a D latch and a D flip-flop, while **Figure Q4(d)(ii)** shows the waveform for signal *CLK* and *D*. Complete the timing diagram for Q_a and Q_b in **APPENDIX A**.

(6 marks)

(e) Design a counter to produce the following sequence of 00, 10, 01, 11, 00...using J-K flip-flops. Your design should include next-state table, transition table, Karnaugh-map simplification and implementation of logic circuit.

(6 marks)

- **END OF QUESTIONS –**

FINAL EXAMINATION

SEMESTER / SESSION : SEM I / 2019/2020
COURSE : ELECTRONIC DIGIT
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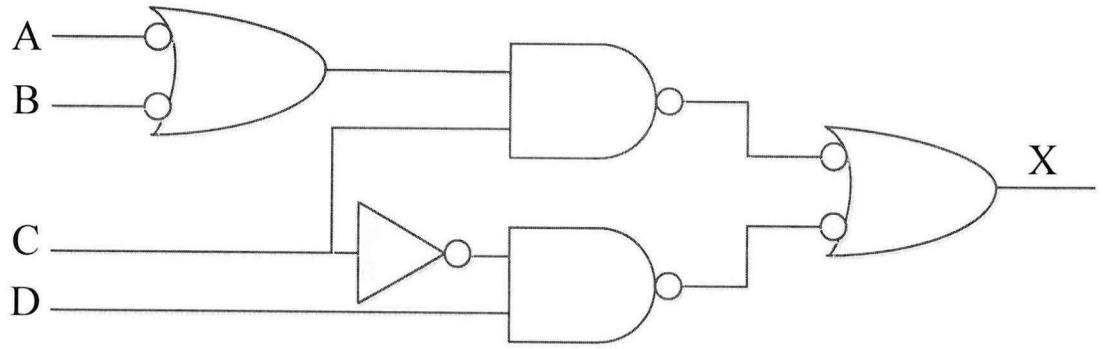

Figure Q1(d)

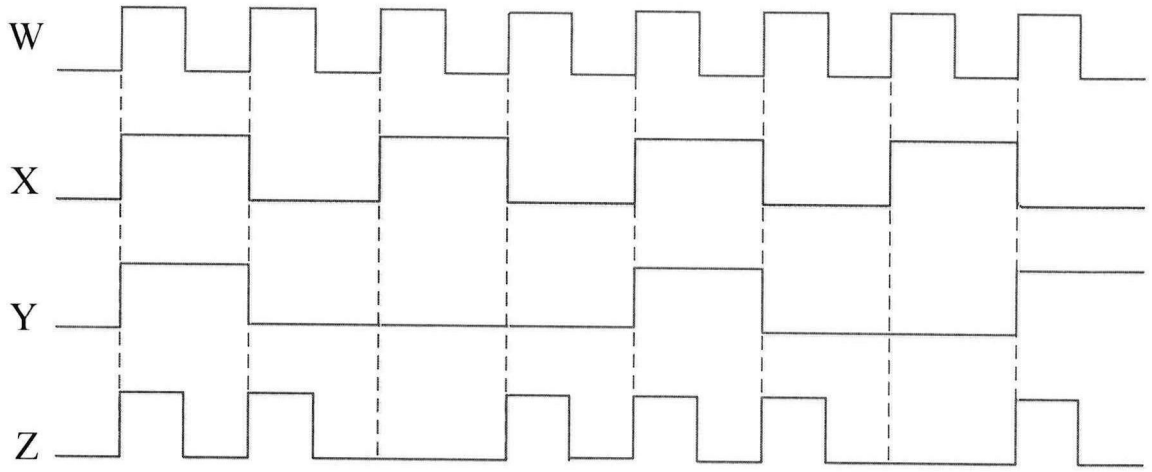

Figure Q2(c)

FINAL EXAMINATION

SEMESTER / SESSION : SEM I / 2019/2020
COURSE : ELECTRONIC DIGIT
PROGRAMME : BND
COURSE CODE : BNR 25402

Table Q3(b)

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

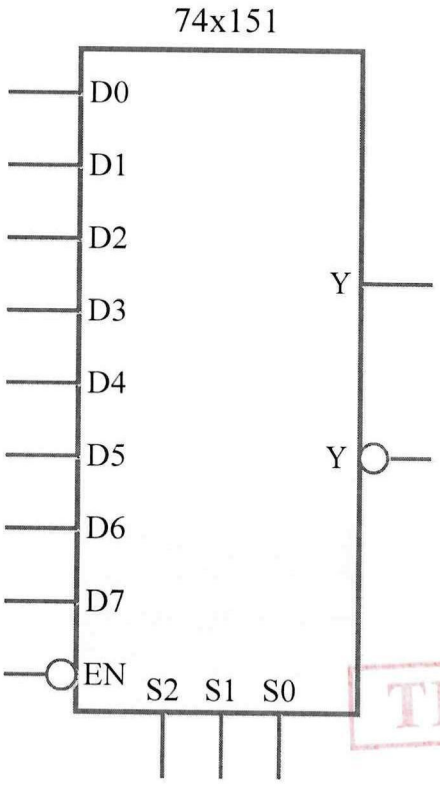

Figure Q3(b)

FINAL EXAMINATION

SEMESTER / SESSION : SEM I / 2019/2020
COURSE : ELECTRONIC DIGIT
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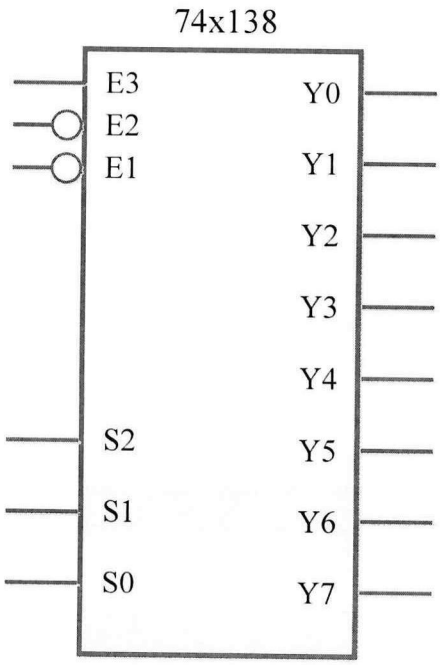

Figure Q3(c)

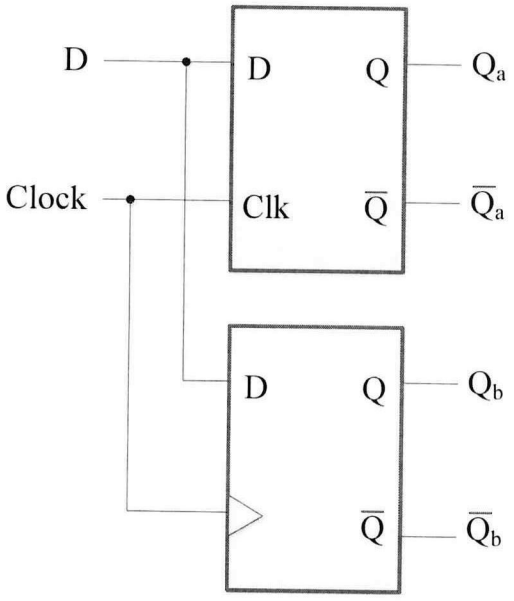

Figure Q4(d)(i)

FINAL EXAMINATION

SEMESTER / SESSION : SEM I / 2019/2020
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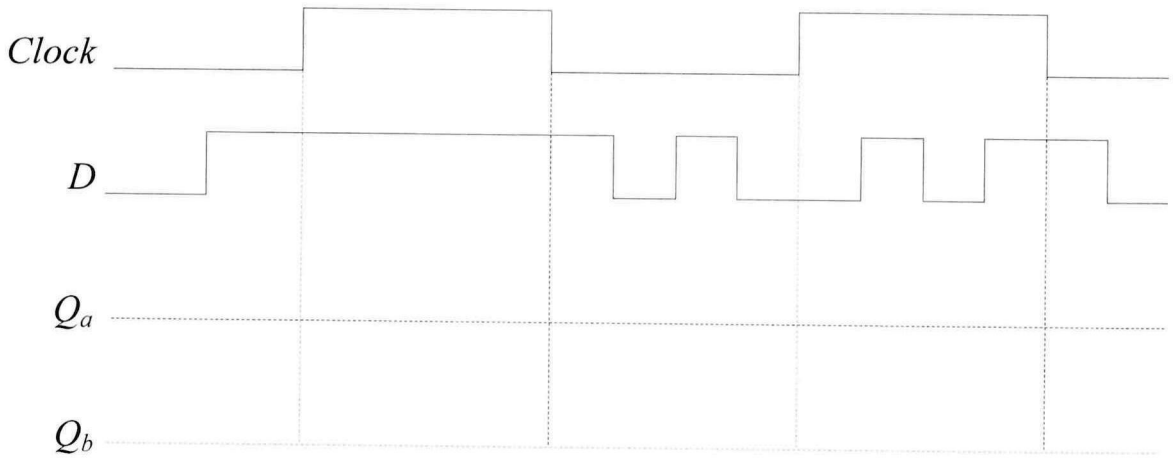

Figure Q4(d)(ii)

FINAL EXAMINATION

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APPENDIX A

NAME : _____

MATRIC NO. : _____