Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2019/2020

COURSE NAME	:	DIGITAL DEVICES AND CIRCUITS
COURSE CODE	:	BNR 23103
PROGRAMME CODE	:	BNE
EXAMINATION DATE	:	DECEMBER 2019 / JANUARY 2020
DURATION	:	3 HOURS
INSTRUCTION	:	1. ANSWER **ALL** QUESTIONS 2. ATTACH **APPENDIX A** WITH YOUR ANSWER BOOKLET

THIS QUESTION PAPER CONSISTS OF **EIGHT (8)** PAGES

Q1 (a) Identify each as digital or analog representation:

(i) Current flowing from an electrical outlet through a motor.
(1 mark)

(ii) Time of day using your cell phone.
(1 mark)

(iii) Volume level of your flat-screen television.
(1 mark)

(iv) Height of a child measured by putting a mark on the wall.
(1 mark)

(b) Give the next number in each of the following sequences:

(i) Gray code : 1010, 1011, ...
(2 marks)

(ii) Hexadecimal : 9FE, 9FF, ...
(2 marks)

(iii) BCD : 10011000, 10011001, ...
(2 marks)

(c) Perform the following operation and provide answer in hexadecimal.

(i) Unsigned number 101110100_2 divide by 2_{10}.
(2 marks)

(ii) $65_{10} - 32_{10}$ in 2's complement.
(3 marks)

(iii) $26A_{16} - 8AF_{16}$.
(2 marks)

(d) Arrange the following numbers in descending order:

$(43)_8$, $(00110111)_{BCD}$, $(24)_{16}$, $(00100010)_2$, $(0201)_4$, $(100110)_{Gray\ Code}$
(4 marks)

(e) Numbers are entered into a microcontroller-based system in BCD, but stored in straight binary. As a programmer, you must decide whether you need a one-byte or two-bytes storage location. Give a reason to prove your answer.

(i) If the system takes a two digits decimal entry.
(2 marks)

(ii) If you want to enter three digits decimal entry.
(2 marks)

Q2 (a) With the aid of diagram, describe the application of AND and OR logic gates used in real life.

(6 marks)

(b) For the following Boolean expression:

$$f(a,b,c,d) = \overline{(abcd + ab\overline{cd} + \overline{ab}cd)}(\bar{c} + \bar{d})(\bar{a} + \bar{b} + c)$$

(i) Simplify it using De Morgan Theorem.

(2 marks)

(ii) From **Q2 (b)(i)**, simplify it using Boolen algebra and verify the answer using a Karnaugh Map.

(4 marks)

(c) The input (*M, N, P*) and output (*Q*) waveforms are applied to a logic circuit as shown in **Figure Q2 (c)**.

(i) Obtain the truth table and Boolean expression of the logic circuit.

(3 marks)

(ii) Simplify the expression and implement the logic circuit using NAND gates ONLY.

(4 marks)

(d) Consider a 3 input truth table which has high values for the output in rows 1, 5 and 7. In this design, you are required to use 2 input NAND gates only and the inputs are available in their true form. Find the total numbers of gates would you need to implement in the circuit if:

(i) you built it directly from the expression in the truth table.

(3 marks)

(ii) you built the minimum SOP realization from a K-map.

(3 marks)

Q3 (a) Give **FOUR (4)** examples of combinational logic functions and explain briefly their function.

(4 marks)

(b) A 6-bit subtractor can be built using the 6-bit ripple adder and 6 inverters. Demonstrate the subtraction of 57_{10} and 22_{10} using the adder.

(4 marks)

(c) For the 4-bit comparator in **Figure Q3 (c)**, plot each output waveform for the inputs shown. The outputs are active-HIGH. Please plot your answer in **Appendix A**.

(3 marks)

(d) Given the following standard SOP Boolean function $F(D, E, F, G) = \Pi (0, 2, 5, 6, 7, 8, 9, 10)$, whereby D is the Most Significant Bit (MSB).

(i) Obtain a truth table for the Boolean function given.

(2 marks)

(ii) Get the expression and implement the circuit using basic logic gate.

(4 marks)

(iii) Draw the gate using a 4:1 multiplexer, a NOR gate and an AND gate ONLY.

(4 marks)

(iv) Draw the gate using a 8:1 multiplexer and an inverter ONLY.

(4 marks)

Q4 (a) State **TWO (2)** differences between sequential logic circuits and combinational logic circuits.

(4 marks)

(b) With the aid of timing diagram, describe how a D latch operates differently from an edge triggered D flip-flop.

(4 marks)

(c) An analogy for a shift register is a conveyor belt as shown in **Figure Q4 (c)**. The illustration showing a single conveyor belt at four different times. State and explain which shift register operations of the following sequence represents.

(4 marks)

(d) Design a 3 bits counter which counts in the sequence 001, 011, 010, 110, 111, 101, 001 using clocked D flip-flops. Your design should include next-state table, transition table, Karnaugh-map simplification and implementation of logic circuit.

(8 marks)

(e) Draw the Mealy state diagram for the **Table Q4 (e)** that describes a finite-state machine which has one input (X) and one output (Z).

(5 marks)

- END OF QUESTIONS -

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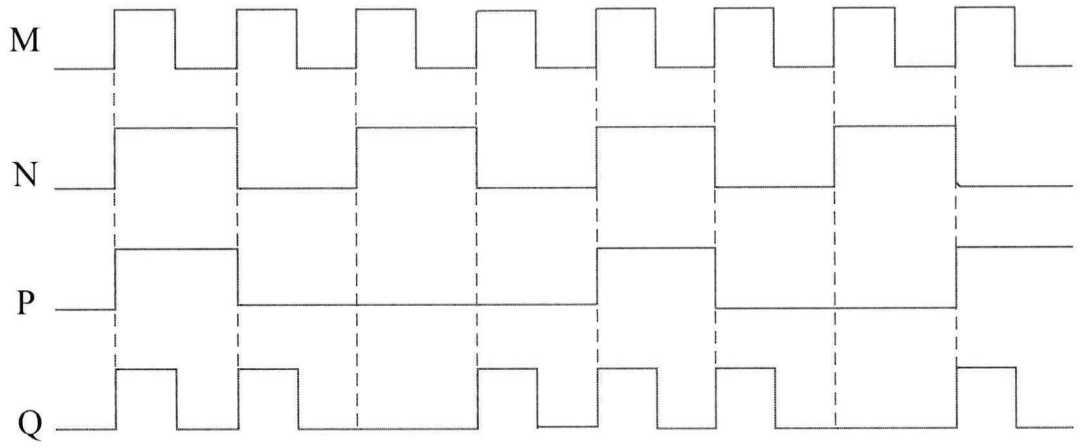

Figure Q2 (c)

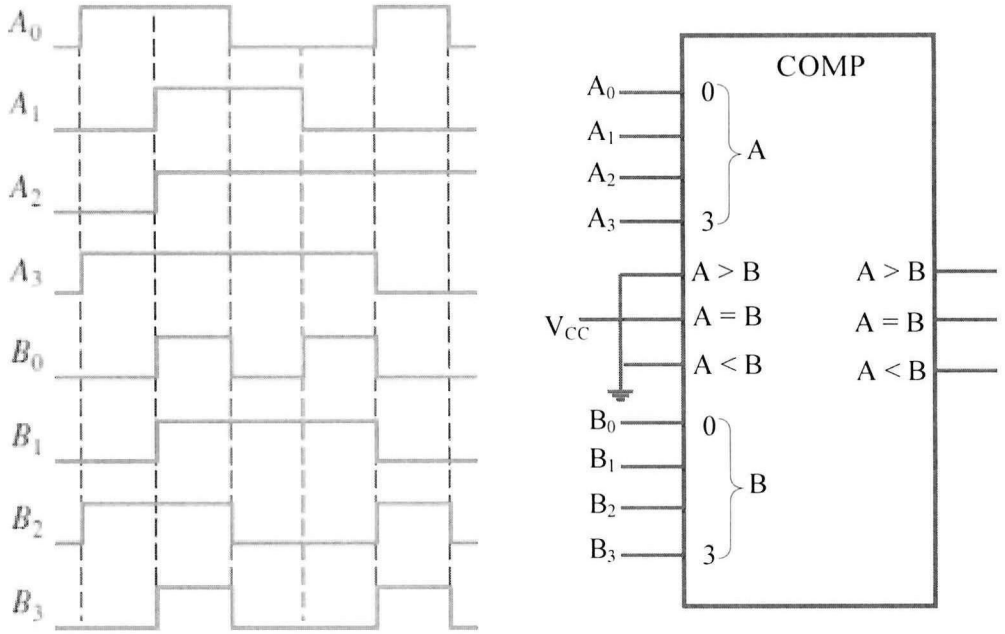

Figure Q3 (c)

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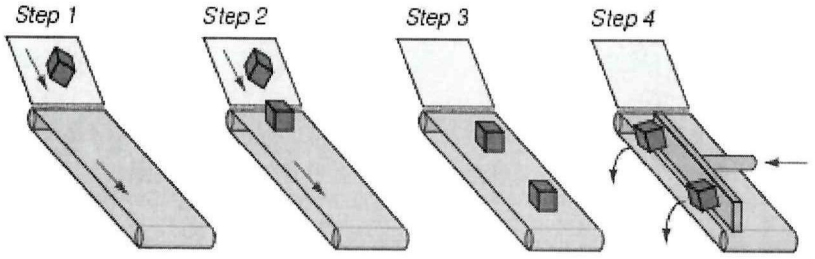
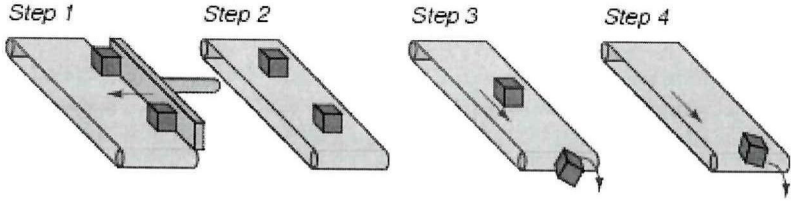


(i)



(ii)

Figure Q4 (c)

Table Q4 (e)

Present State	Next State		Output (Z)	
	X = 0	X = 1	X = 0	X = 1
A	A	E	1	0
B	C	F	0	0
C	B	H	0	1
D	E	F	0	0
E	D	A	0	1
F	B	F	1	1
G	D	H	0	1
H	H	G	1	0

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APPENDIX A

NAME : _____

MATRIC NO. : _____