Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2019/2020

COURSE NAME	:	COMPUTER ARCHITECTURE
COURSE CODE	:	BNF 31802
PROGRAMME CODE	:	BNF
EXAMINATION DATE	:	DECEMBER 2019 / JANUARY 2020
DURATION	:	2 HOURS
INSTRUCTION	:	ANSWER **ALL** QUESTIONS

THIS QUESTION PAPER CONSISTS OF **FIVE (5)** PAGES

Q1 (a) What is computer architecture and organization?

(4 marks)

(b) Consider two different machines, with two different instruction sets, both of which having a clock rate of 200 MHz. The measurements in **Table Q1(b)** are recorded on the two machines running a given set of benchmark programs. Given

$$CPI = \frac{\sum_{i=1}^{n}(CPI_i \times I_i)}{I_c}$$

$$MIPS\ rate = \frac{I_c}{T \times 10^6} = \frac{f}{CPI \times 10^6}$$

(i) Determine the effective CPI, MIPS rate, and execution time for each machine.

(6 marks)

(ii) Analyse the results.

(2 marks)

(c) Four benchmark programs are executed on three computers. **Table Q1(c)** shows the execution time in seconds, with 100,000,000 instructions executed in each of the four programs.

(i) Calculate the MIPS values for each computer for each program.

(4 marks)

(ii) Calculate the arithmetic and harmonic means assuming equal weights for the four programs, and rank the computers based on arithmetic mean and harmonic mean.

(4 marks)

Q2 (a) Explain the differences among direct mapping, associative mapping, and set associative mapping.

(6 marks)

(b) A set-associative cache consists of 64 lines, or slots, divided into four-line sets. Main memory contains 4K blocks of 128 words each. Show the format of main memory addresses.

(4 marks)

(c) Consider a machine with a byte addressable main memory of 2^{16} bytes and block size of 8 bytes. Assume that a direct mapped cache consisting of 32 lines is used with this machine.

(i) Show how is a 16-bit memory address divided into tag, line number, and byte number.

(2 marks)

(ii) Determine into what line would bytes with each of the following addresses be stored

0001 0001 0001 1011
1100 0011 0011 0100
1101 0000 0001 1101
1010 1010 1010 1010

(2 marks)

(iii) Suppose the byte with address 0001 1010 0001 1010 is stored in the cache. Determine the addresses of the other bytes stored along with it.

(2 marks)

(iv) Determine the total bytes of memory can be stored in the cache.

(2 marks)

(v) Explain why is the tag also stored in the cache.

(2 marks)

Q3 (a) Explain Direct Memory Access (DMA) operation.

(4 marks)

(b) Discuss **THREE (3)** functions of Operating System.

(6 marks)

(c) (i) State **FOUR (4)** types of Operating System.

(4 marks)

(ii) Differentiate between single programming operation and multi-programming operation. Sketch the diagram.

(6 marks)

Q4 (a) Explain the the process accessing MIPS memory from and to register.

(6 marks)

(b) Identify an assembly code based on program below.

(7 marks)

```
        i = -1 ;
Loop:   i = i + 1 ;
        if i > 39, then goto Exit ;

        temp1 = 2 * i ;
        offset = temp1 + temp1 ;
        addr = baseaddr + offset ;
        load temp3 from M(addr) ;
        temp4 = temp1 – temp3 ;
        store temp4 at M(addr) ;
        goto    Loop ;
Exit: ...
```

(c) Explain the MIPS addressing mode (R, I, J) is used for, and give one example of each mode

(7 marks)

Q5 (a) Sketch MIPS Pipeline processor and explain briefly each parts.

(8 marks)

(b) The following MIPS program is to be run on a MIPS pipeline processor of form IF-ID-EX-MEM-WB. Please identify all data dependencies beside each instruction

```
L_1 lw $t2, 60($t1)
L_2 lw $t1, 40($t2)
L_3 slt $t1, $t1, $t2
L_4 sw $t1, 20($t2)
```

(6 marks)

(c) Identify the optimal pipeline schedule using forwarding from EX or MEM stages to any other stage, then compute the pipeline CPI base on instruction below.

```
L_1 lw $t2, 60($t1)
L_2 lw $t1, 40($t2)
L_3 slt $t1, $t1, $t2
L_4 sw $t1, 20($t2)
```

(6 marks)

- END OF QUESTIONS -

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Table Q1(b)

	Instruction Type	Instruction Count (millions)	Cycles per Instruction
Machine A	Arithmetic and logic	8	1
	Load and store	4	3
	Branch	2	4
	Others	4	3
Machine B	Arithmetic and logic	10	1
	Load and store	8	2
	Branch	2	4
	Others	4	3

Table Q1(c)

Type of Program	Computer A	Computer B	Computer C
Program 1	1	10	20
Program 2	1000	100	20
Program 3	500	1000	50
Program 4	100	800	100