UTHM
Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2019/2020

COURSE NAME	:	MICROCONTROLLER APPLICATION
COURSE CODE	:	BNR 35503/BND 35503/BNR 36603
PROGRAMME CODE	:	BND/BNE
EXAMINATION DATE	:	DECEMBER 2019/JANUARY 2020
DURATION	:	2 HOURS 30 MINUTES
INSTRUCTION	:	ANSWER **ALL** QUESTIONS

TERBUKA

THIS QUESTION PAPER CONSISTS OF **FIFTEEN (15)** PAGES

Q1 (a) A microcontroller application PIC18F4550 require an external push button to trigger an interrupt routine. Name the interrupt source and suggest a suitable value for INTCON.

(4 marks)

(b) Given the clock input for the PIC18F4550 is 10 MHz. Calculate the value to be loaded into TMR0 registers <TMR0H:TMR0L> based on 16 bit timer configuration and suggest a suitable prescale value to create 1s delay.

(8 marks)

(c) Suggest and explain the value of INTCON register if the specifications are as in question **Q1(b)**.

(4 marks)

(d) If the PIC 18F4550 is connected to a LED as shown in **Figure Q1(d)**. Write a simple program to blink the LED every 2s (1s ON, 1s OFF) using specifications as in question **Q1(b)**.

(7 marks)

(e) Suggest **ONE(1)** other application for the code written in question **Q1(d)** besides LED blinking.

(2 marks)

Q2 **Figure Q2** shows a simple circuit diagram using PIC 18F4550 with two analog input via RA0 and RA1 pins. There are two LEDs, LED1 and LED2 connected to RB0 and RB1 respectively. RB2 is connected to another output called output 1. The PIC is clocked at 20MHz.

(a) Based on the circuit in **Figure Q2,** determine and explain the initialization value of ADCON0 if an application require the system to input a temperature sensor on RA0. Suggest the most suitable value for ADCON1 and ADCON2.

(5 marks)

(b) Write a sequence of C code to initialize the ADC with left-justified output, read analog input from RA0, then light LED1 if analog input value is more than 75%.

(5 marks)

(c) Prepare a simple C code that read analog input from RA0 and transfer ADRESH output into LATC. If the analog value is less than 50%, transfer ADRESH into LATD. (Hint: Make sure ADC configuration registers are set properly)

(6 marks)

(d) Refering to **Figure Q2,** write a simple C program to light the LED1 when the analog value of RA0 is greater than RA1 and light the LED2 when the analog value of RA1 is greater than RA0.

(9 marks)

CONFIDENTIAL

Q3 (a) List **THREE (3)** factors that may affect the speed of a motor.

(3 marks)

(b) Determine a suitable value for PR2 and the prescaler needed to get 4.88 kHz PWM frequency. Assume XTAL = 20 MHz.

(4 marks)

(c) Demonstrate the representation of 75% duty cycle with 4.88 kHz PWM frequency in CCPR1L and CCP1CON register.

(4 marks)

(d) Construct a code for creating alternating square wave of 80% and 20% duty cycle on the PORTB bit 0 with 1s delay between both duty cycles. Timer2 is used to generate the time delay and the PWM frequency is 4.88 kHz.

(14 marks)

Q4 (a) The PIC18 transfers and receives data serially at many different baud rates. The baud rate is reprogrammable with the 8-bit register called SPBRG.

(i) For XTAL = 10 MHz, calculate the SPBRG value (in both decimal and hex) for baud rates 9600.

(3 marks)

(ii) Investigate the SPBRG value (in both decimal and hex) for question **Q4(a)(i)**. Given that the value of BRGH bit of TXSTA register is HIGH.

(3 marks)

(iii) Calculate the baud rate error for question **Q4(a)(i)**.

(3 marks)

(b) Create a C program and draw schematic diagram based on the following specification:

"PIC18 gets analog input from a variable resistor to RA0. 8 LEDs are connected to PORTD and the LEDs sequentially light based on the analog input. (0 LED at 0%, 4LEDs at 50% and 8 LEDs at 100%). A DC motor is connected to RB0 and the speed correspond to the analog input. Assume that XTAL = 10 MHz"

(16 marks)

- **END OF QUESTIONS** -

CONFIDENTIAL

FINAL EXAMINATION

SEMESTER / SESSION	: SEM I / 2019/2020	PROGRAMME CODE	: BND/BNE
COURSE NAME	: MICROCONTROLLER	COURSE CODE	: BNR35503/
	APPLICATION		BND35503/
			BNR36603

Figure Q1(d)

CONFIDENTIAL
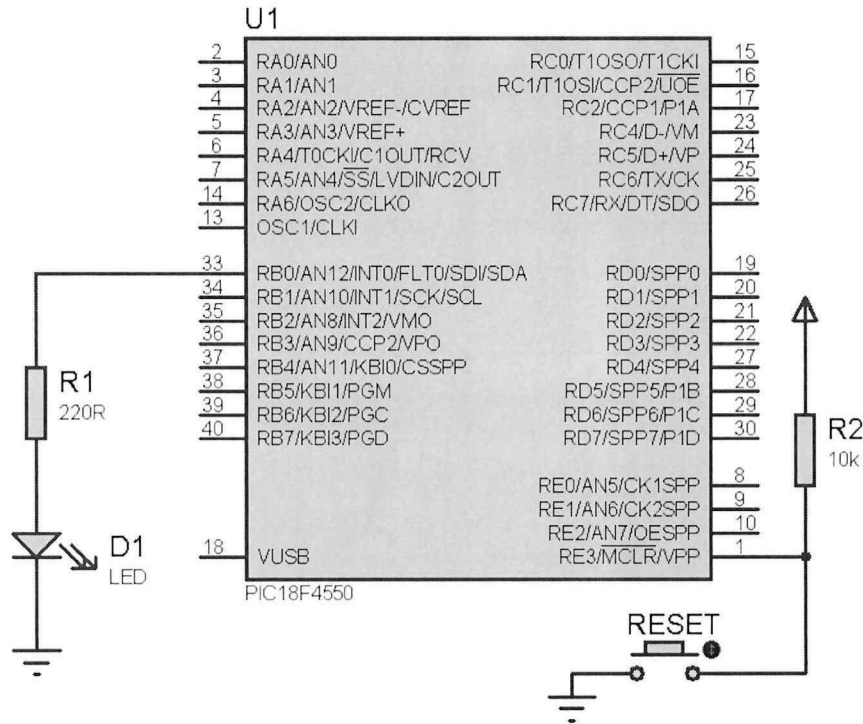
FINAL EXAMINATION

SEMESTER / SESSION   : SEM I / 2019/2020   PROGRAMME CODE   :   BND/BNE
COURSE NAME   : MICROCONTROLLER   COURSE CODE   :   BNR35503/
                        APPLICATION   BND35503/
                                                                       BNR36603
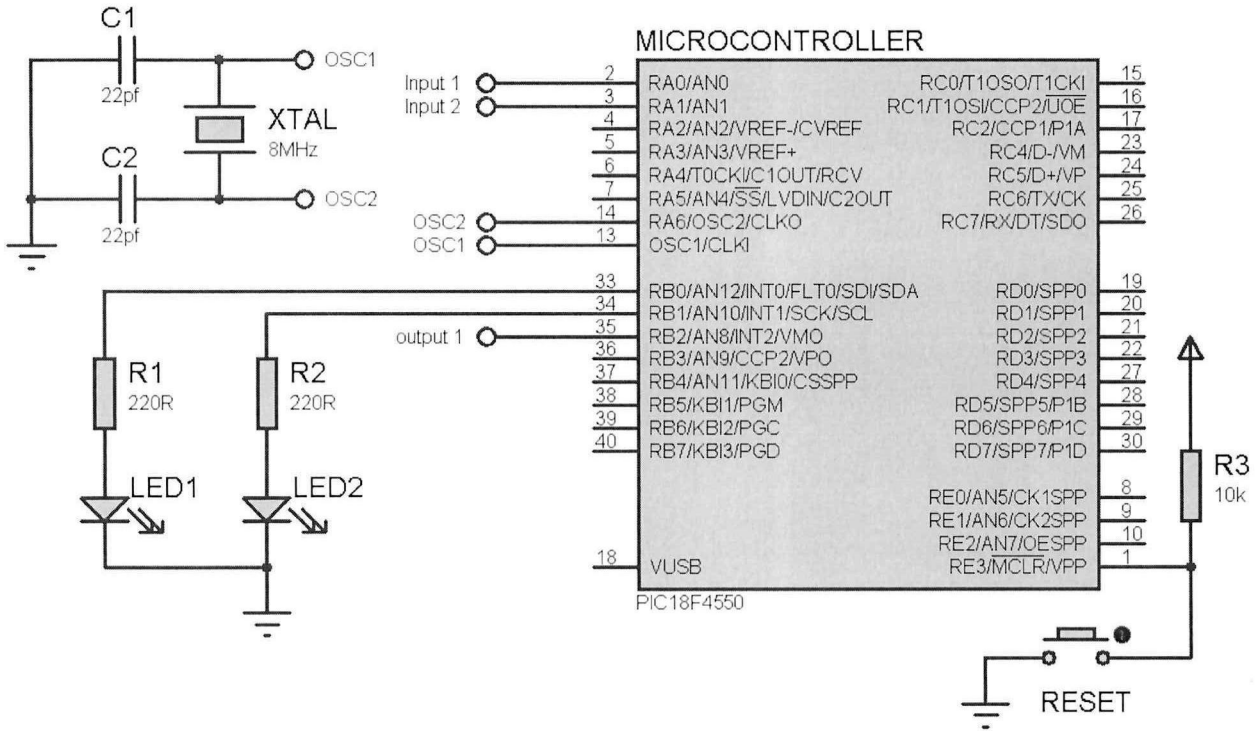
Figure Q2

FINAL EXAMINATION

SEMESTER / SESSION : SEM I / 2019/2020	PROGRAMME CODE : BND/BNE
COURSE NAME : MICROCONTROLLER APPLICATION	COURSE CODE : BNR35503/ BND35503/ BNR36603

APPENDIX I : SPECIAL FUNCTION REGISTER (SFR)

Address	Name	Address	Name	Address	Name	Address	Name	Address	Name
FFFh	TOSU	FDFh	INDF2[1]	FBFh	CCPR1H	F9Fh	IPR1	F7Fh	UEP15
FFEh	TOSH	FDEh	POSTINC2[1]	FBEh	CCPR1L	F9Eh	PIR1	F7Eh	UEP14
FFDh	TOSL	FDDh	POSTDEC2[1]	FBDh	CCP1CON	F9Dh	PIE1	F7Dh	UEP13
FFCh	STKPTR	FDCh	PREINC2[1]	FBCh	CCPR2H	F9Ch	—[2]	F7Ch	UEP12
FFBh	PCLATU	FDBh	PLUSW2[1]	FBBh	CCPR2L	F9Bh	OSCTUNE	F7Bh	UEP11
FFAh	PCLATH	FDAh	FSR2H	FBAh	CCP2CON	F9Ah	—[2]	F7Ah	UEP10
FF9h	PCL	FD9h	FSR2L	FB9h	—[2]	F99h	—[2]	F79h	UEP9
FF8h	TBLPTRU	FD8h	STATUS	FB8h	BAUDCON	F98h	—[2]	F78h	UEP8
FF7h	TBLPTRH	FD7h	TMR0H	FB7h	ECCP1DEL	F97h	—[2]	F77h	UEP7
FF6h	TBLPTRL	FD6h	TMR0L	FB6h	ECCP1AS	F96h	TRISE[3]	F76h	UEP6
FF5h	TABLAT	FD5h	T0CON	FB5h	CVRCON	F95h	TRISD[3]	F75h	UEP5
FF4h	PRODH	FD4h	—[2]	FB4h	CMCON	F94h	TRISC	F74h	UEP4
FF3h	PRODL	FD3h	OSCCON	FB3h	TMR3H	F93h	TRISB	F73h	UEP3
FF2h	INTCON	FD2h	HLVDCON	FB2h	TMR3L	F92h	TRISA	F72h	UEP2
FF1h	INTCON2	FD1h	WDTCON	FB1h	T3CON	F91h	—[2]	F71h	UEP1
FF0h	INTCON3	FD0h	RCON	FB0h	SPBRGH	F90h	—[2]	F70h	UEP0
FEFh	INDF0[1]	FCFh	TMR1H	FAFh	SPBRG	F8Fh	—[2]	F6Fh	UCFG
FEEh	POSTINC0[1]	FCEh	TMR1L	FAEh	RCREG	F8Eh	—[2]	F6Eh	UADDR
FEDh	POSTDEC0[1]	FCDh	T1CON	FADh	TXREG	F8Dh	LATE[3]	F6Dh	UCON
FECh	PREINC0[1]	FCCh	TMR2	FACh	TXSTA	F8Ch	LATD[3]	F6Ch	USTAT
FEBh	PLUSW0[1]	FCBh	PR2	FABh	RCSTA	F8Bh	LATC	F6Bh	UEIE
FEAh	FSR0H	FCAh	T2CON	FAAh	—[2]	F8Ah	LATB	F6Ah	UEIR
FE9h	FSR0L	FC9h	SSPBUF	FA9h	EEADR	F89h	LATA	F69h	UIE
FE8h	WREG	FC8h	SSPADD	FA8h	EEDATA	F88h	—[2]	F68h	UIR
FE7h	INDF1[1]	FC7h	SSPSTAT	FA7h	EECON2[1]	F87h	—[2]	F67h	UFRMH
FE6h	POSTINC1[1]	FC6h	SSPCON1	FA6h	EECON1	F86h	—[2]	F66h	UFRML
FE5h	POSTDEC1[1]	FC5h	SSPCON2	FA5h	—[2]	F85h	—[2]	F65h	SPPCON[3]
FE4h	PREINC1[1]	FC4h	ADRESH	FA4h	—[2]	F84h	PORTE	F64h	SPPEPS[3]
FE3h	PLUSW1[1]	FC3h	ADRESL	FA3h	—[2]	F83h	PORTD[3]	F63h	SPPCFG[3]
FE2h	FSR1H	FC2h	ADCON0	FA2h	IPR2	F82h	PORTC	F62h	SPPDATA[3]
FE1h	FSR1L	FC1h	ADCON1	FA1h	PIR2	F81h	PORTB	F61h	—[2]
FE0h	BSR	FC0h	ADCON2	FA0h	PIE2	F80h	PORTA	F60h	—[2]

CONFIDENTIAL

FINAL EXAMINATION

SEMESTER / SESSION	: SEM I / 2019/2020	PROGRAMME CODE	: BND/BNE
COURSE NAME	: MICROCONTROLLER APPLICATION	COURSE CODE	: BNR35503/ BND35503/ BNR36603

APPENDIX II : INTERRUPT CONTROL REGISTER (INTCON)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF[1]
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared　　x = Bit is unknown

bit 7　　**GIE/GIEH:** Global Interrupt Enable bit

When IPEN = 0:
1 = Enables all unmasked interrupts
0 = Disables all interrupts

When IPEN = 1:
1 = Enables all high-priority interrupts
0 = Disables all interrupts

bit 6　　**PEIE/GIEL:** Peripheral Interrupt Enable bit

When IPEN = 0:
1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts

When IPEN = 1:
1 = Enables all low-priority peripheral interrupts (if GIE/GIEH = 1)
0 = Disables all low-priority peripheral interrupts

bit 5　　**TMR0IE:** TMR0 Overflow Interrupt Enable bit

1 = Enables the TMR0 overflow interrupt
0 = Disables the TMR0 overflow interrupt

bit 4　　**INT0IE:** INT0 External Interrupt Enable bit

1 = Enables the INT0 external interrupt
0 = Disables the INT0 external interrupt

bit 3　　**RBIE:** RB Port Change Interrupt Enable bit

1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

bit 2　　**TMR0IF:** TMR0 Overflow Interrupt Flag bit

1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

bit 1　　**INT0IF:** INT0 External Interrupt Flag bit

1 = The INT0 external interrupt occurred (must be cleared in software)
0 = The INT0 external interrupt did not occur

bit 0　　**RBIF:** RB Port Change Interrupt Flag bit[1]

1 = At least one of the RB7:RB4 pins changed state (must be cleared in software)
0 = None of the RB7:RB4 pins have changed state

FINAL EXAMINATION

SEMESTER / SESSION	: SEM I / 2019/2020	PROGRAMME CODE : BND/BNE
COURSE NAME	: MICROCONTROLLER	COURSE CODE : BNR35503/
	APPLICATION	BND35503/
		BNR36603

APPENDIX III : TIMER0 CONTROL REGISTER (T0CON)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
TMR0ON	T08BIT	T0CS	T0SE	PSA	T0PS2	T0PS1	T0PS0
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 7   **TMR0ON:** Timer0 On/Off Control bit

                     1 = Enables Timer0
                     0 = Stops Timer0

bit 6   **T08BIT**: Timer0 8-Bit/16-Bit Control bit

                     1 = Timer0 is configured as an 8-bit timer/counter
                     0 = Timer0 is configured as a 16-bit timer/counter

bit 5   **T0CS**: Timer0 Clock Source Select bit

                     1 = Transition on T0CKI pin
                     0 = Internal instruction cycle clock (CLKO)

bit 4   **T0SE**: Timer0 Source Edge Select bit

                     1 = Increment on high-to-low transition on T0CKI pin
                     0 = Increment on low-to-high transition on T0CKI pin

bit 3   **PSA**: Timer0 Prescaler Assignment bit

                     1 = TImer0 prescaler is NOT assigned. Timer0 clock input bypasses prescaler.
                     0 = Timer0 prescaler is assigned. Timer0 clock input comes from prescaler output.

bit 2-0   **T0PS2:T0PS0**: Timer0 Prescaler Select bits

                     111 = 1:256 Prescale value
                     110 = 1:128 Prescale value
                     101 = 1:64   Prescale value
                     100 = 1:32   Prescale value
                     011 = 1:16   Prescale value
                     010 = 1:8   Prescale value
                     001 = 1:4   Prescale value
                     000 = 1:2   Prescale value

FINAL EXAMINATION

| SEMESTER / SESSION | : SEM I / 2019/2020 | PROGRAMME CODE | : BND/BNE |
| COURSE NAME | : MICROCONTROLLER APPLICATION | COURSE CODE | : BNR35503/ BND35503/ BNR36603 |

APPENDIX IV : A/D CONTROL REGISTER 0 (ADCON0)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CHS3	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 7-6   **Unimplemented:** Read as '0'

bit 5-2   **CHS3:CHS0:** Analog Channel Select bits
$\quad$ 0000 = Channel 0 (AN0)
$\quad$ 0001 = Channel 1 (AN1)
$\quad$ 0010 = Channel 2 (AN2)
$\quad$ 0011 = Channel 3 (AN3)
$\quad$ 0100 = Channel 4 (AN4)
$\quad$ 0101 = Channel 5 (AN5)[1,2]
$\quad$ 0110 = Channel 6 (AN6)[1,2]
$\quad$ 0111 = Channel 7 (AN7)[1,2]
$\quad$ 1000 = Channel 8 (AN8)
$\quad$ 1001 = Channel 9 (AN9)
$\quad$ 1010 = Channel 10 (AN10)
$\quad$ 1011 = Channel 11 (AN11)
$\quad$ 1100 = Channel 12 (AN12)
$\quad$ 1101 = Unimplemented[2]
$\quad$ 1110 = Unimplemented[2]
$\quad$ 1111 = Unimplemented[2]

bit 1   **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit
$\quad$ When ADON = 1:
$\quad$ 1 = A/D conversion in progress
$\quad$ 0 = A/D Idle

bit 0   **ADON:** A/D On bit
$\quad$ 1 = A/D converter module is enabled
$\quad$ 0 = A/D converter module is disabled

CONFIDENTIAL

FINAL EXAMINATION

SEMESTER / SESSION	: SEM I / 2019/2020	PROGRAMME CODE : BND/BNE
COURSE NAME	: MICROCONTROLLER APPLICATION	COURSE CODE : BNR35503/ BND35503/ BNR36603

APPENDIX V : A/D CONTROL REGISTER 1 (ADCON1)

U-0	U-0	R/W-0	R/W-0	R/W-0[1]	R/W[1]	R/W[1]	R/W[1]
—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 7-6   **Unimplemented:** Read as '0'

bit 5   **VCFG1:** Voltage Reference Configuration bit (V_{REF}- source)

       $1 = V_{REF}$- (AN2)

       $0 = V_{SS}$

bit 4   **VCFG0:** Voltage Reference Configuration bit (V_{REF}+ source)

       $1 = V_{REF}$+ (AN3)

       $0 = V_{DD}$

bit 3-0   **PCFG3:PCFG0:** A/D Port Configuration Control bits:

PCFG3: PCFG0	AN12	AN11	AN10	AN9	AN8	AN7[2]	AN6[2]	AN5[2]	AN4	AN3	AN2	AN1	AN0
0000[1]	A	A	A	A	A	A	A	A	A	A	A	A	A
0001	A	A	A	A	A	A	A	A	A	A	A	A	A
0010	A	A	A	A	A	A	A	A	A	A	A	A	A
0011	D	A	A	A	A	A	A	A	A	A	A	A	A
0100	D	D	A	A	A	A	A	A	A	A	A	A	A
0101	D	D	D	A	A	A	A	A	A	A	A	A	A
0110	D	D	D	D	A	A	A	A	A	A	A	A	A
0111[1]	D	D	D	D	D	A	A	A	A	A	A	A	A
1000	D	D	D	D	D	D	A	A	A	A	A	A	A
1001	D	D	D	D	D	D	D	A	A	A	A	A	A
1010	D	D	D	D	D	D	D	D	A	A	A	A	A
1011	D	D	D	D	D	D	D	D	D	A	A	A	A
1100	D	D	D	D	D	D	D	D	D	D	A	A	A
1101	D	D	D	D	D	D	D	D	D	D	D	A	A
1110	D	D	D	D	D	D	D	D	D	D	D	D	A
1111	D	D	D	D	D	D	D	D	D	D	D	D	D

A = Analog input   D = Digital I/O

CONFIDENTIAL

FINAL EXAMINATION

SEMESTER / SESSION	: SEM I / 2019/2020	PROGRAMME CODE	: BND/BNE
COURSE NAME	: MICROCONTROLLER APPLICATION	COURSE CODE	: BNR35503/ BND35503/ BNR36603

APPENDIX VI : A/D CONTROL REGISTER 2 (ADCON2)

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 7   **ADFM:** A/D Result Format Select bit

1 = Right justified
0 = Left justified

bit 6   **Unimplemented:** Read as '0'

bit 5-3   **ACQT2:ACQT0:** A/D Acquisition Time Select bits

$111 = 20\ T_{AD}$
$110 = 16\ T_{AD}$
$101 = 12\ T_{AD}$
$100 = 8\ T_{AD}$
$011 = 6\ T_{AD}$
$010 = 4\ T_{AD}$
$001 = 2\ T_{AD}$
$000 = 0\ T_{AD}$[1]

bit 2-0   **ADCS2:ADCS0:** A/D Conversion Clock Select bits

111 = F_{RC} (clock derived from A/D RC oscillator)[1]
110 = Fosc/64
101 = Fosc/16
100 = Fosc/4
011 = F_{RC} (clock derived from A/D RC oscillator)[1]
010 = Fosc/32
001 = Fosc/8
000 = Fosc/2

FINAL EXAMINATION

SEMESTER / SESSION	: SEM I / 2019/2020	PROGRAMME CODE	: BND/BNE
COURSE NAME	: MICROCONTROLLER APPLICATION	COURSE CODE	: BNR35503/ BND35503/ BNR36603

APPENDIX VII : ECCP CONTROL REGISTER (CCP1CON)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
P1M1	P1M0	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0

bit 7   bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6   **P1M1:P1M0**: Enhanced PWM Output Configuration bits

             If CCP1M3:CCP1M2 = 00, 01, 10:
             xx = P1A assigned as Capture/Compare input/output; P1B, P1C, P1D assigned as port pins
             If CCP1M3:CCP1M2 = 11:
             00 = Single output: P1A modulated; P1B, P1C, P1D assigned as port pins
             01 = Full-bridge output forward: P1D modulated; P1A active; P1B, P1C inactive
             10 = Half-bridge output: P1A, P1B modulated with dead-band control; P1C, P1D assigned as port pins
             11 = Full-bridge output reverse: P1B modulated; P1C active; P1A, P1D inactive

bit 5-4   **DC1B1:DC1B0**: PWM Duty Cycle Bit 1 and Bit 0

             Capture mode:
             Unused.

             Compare mode:
             Unused.

             PWM mode:
             These bits are the two LSbs of the 10-bit PWM duty cycle. The eight MSbs of the duty cycle are found in CCPR1L.

bit 3-0   **CCP1M3:CCP1M0**: Enhanced CCP Mode Select bits

             0000 = Capture/Compare/PWM off (resets ECCP module)
             0001 = Reserved
             0010 = Compare mode, toggle output on match
             0011 = Capture mode
             0100 = Capture mode, every falling edge
             0101 = Capture mode, every rising edge
             0110 = Capture mode, every 4th rising edge
             0111 = Capture mode, every 16th rising edge
             1000 = Compare mode, initialize CCP1 pin low, set output on compare match (set CCP1IF)
             1001 = Compare mode, initialize CCP1 pin high, clear output on compare match (set CCP1IF)
             1010 = Compare mode, generate software interrupt only, CCP1 pin reverts to I/O state
             1011 = Compare mode, trigger special event (CCP1 resets TMR1 or TMR3, sets CCP1IF bit)
             1100 = PWM mode: P1A, P1C active-high; P1B, P1D active-high
             1101 = PWM mode: P1A, P1C active-high; P1B, P1D active-low
             1110 = PWM mode: P1A, P1C active-low; P1B, P1D active-high
             1111 = PWM mode: P1A, P1C active-low; P1B, P1D active-low

CONFIDENTIAL

FINAL EXAMINATION

SEMESTER / SESSION	: SEM I / 2019/2020	PROGRAMME CODE	: BND/BNE
COURSE NAME	: MICROCONTROLLER APPLICATION	COURSE CODE	: BNR35503/ BND35503/ BNR36603

APPENDIX VIII : TRANSMIT STATUS AND CONTROL REGISTER (TXSTA)

REGISTER 20-1:   TXSTA: TRANSMIT STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-1	R/W-0
CSRC	TX9	TXEN[1]	SYNC	SENDB	BRGH	TRMT	TX9D
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7   **CSRC: Clock Source Select bit**

Asynchronous mode:
Don't care.

Synchronous mode:
1 = Master mode (clock generated internally from BRG)
0 = Slave mode (clock from external source)

bit 6   **TX9: 9-Bit Transmit Enable bit**

1 = Selects 9-bit transmission
0 = Selects 8-bit transmission

bit 5   **TXEN: Transmit Enable bit[1]**

1 = Transmit enabled
0 = Transmit disabled

bit 4   **SYNC: EUSART Mode Select bit**

1 = Synchronous mode
0 = Asynchronous mode

bit 3   **SENDB: Send Break Character bit**

Asynchronous mode:
1 = Send Sync Break on next transmission (cleared by hardware upon completion)
0 = Sync Break transmission completed

Synchronous mode:
Don't care.

bit 2   **BRGH: High Baud Rate Select bit**

Asynchronous mode:
1 = High speed
0 = Low speed

Synchronous mode:
Unused in this mode.

bit 1   **TRMT: Transmit Shift Register Status bit**

1 = TSR empty
0 = TSR full

bit 0   **TX9D: 9th bit of Transmit Data**
Can be address/data bit or a parity bit.

Note 1:   SREN/CREN overrides TXEN in Sync mode with the exception that SREN has no effect in Synchronous Slave mode.

FINAL EXAMINATION

SEMESTER / SESSION	: SEM I / 2019/2020	PROGRAMME CODE	: BND/BNE
COURSE NAME	: MICROCONTROLLER	COURSE CODE	: BNR35503/
	APPLICATION		BND35503/
			BNR36603

APPENDIX IX : RECEIVE STATUS AND CONTROL REGISTER (RCSTA)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-x
SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D

bit 7　　　　　　　　　　　　　　　　　　　　　　　　　　　　　　　　　　　　　　bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7　　　**SPEN:** Serial Port Enable bit

1 = Serial port enabled (configures RX/DT and TX/CK pins as serial port pins)
0 = Serial port disabled (held in Reset)

bit 6　　　**RX9:** 9-Bit Receive Enable bit

1 = Selects 9-bit reception
0 = Selects 8-bit reception

bit 5　　　**SREN:** Single Receive Enable bit

Asynchronous mode:
Don't care.

Synchronous mode – Master:
1 = Enables single receive
0 = Disables single receive
This bit is cleared after reception is complete.

Synchronous mode – Slave:
Don't care.

bit 4　　　**CREN:** Continuous Receive Enable bit

Asynchronous mode:
1 = Enables receiver
0 = Disables receiver

Synchronous mode:
1 = Enables continuous receive until enable bit CREN is cleared (CREN overrides SREN)
0 = Disables continuous receive

bit 3　　　**ADDEN:** Address Detect Enable bit

Asynchronous mode 9-bit (RX9 = 1):
1 = Enables address detection, enables interrupt and loads the receive buffer when RSR<8> is set
0 = Disables address detection, all bytes are received and ninth bit can be used as parity bit

Asynchronous mode 8-bit (RX9 = 0):
Don't care.

bit 2　　　**FERR:** Framing Error bit

1 = Framing error (can be updated by reading RCREG register and receiving next valid byte)
0 = No framing error

bit 1　　　**OERR:** Overrun Error bit

1 = Overrun error (can be cleared by clearing bit CREN)
0 = No overrun error

bit 0　　　**RX9D:** 9th bit of Received Data

This can be address/data bit or a parity bit and must be calculated by user firmware.

14

FINAL EXAMINATION

SEMESTER / SESSION	: SEM I / 2019/2020	PROGRAMME CODE	: BND/BNE
COURSE NAME	: MICROCONTROLLER APPLICATION	COURSE CODE	: BNR35503/ BND35503/ BNR36603

APPENDIX X : BAUD RATE CONTROL REGISTER (BAUDCON)

R/W-0	R-1	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
ABDOVF	RCIDL	RXDTP	TXCKP	BRG16	—	WUE	ABDEN
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **ABDOVF:** Auto-Baud Acquisition Rollover Status bit
1 = A BRG rollover has occurred during Auto-Baud Rate Detect mode (must be cleared in software)
0 = No BRG rollover has occurred

bit 6 **RCIDL:** Receive Operation Idle Status bit
1 = Receive operation is Idle
0 = Receive operation is active

bit 5 **RXDTP:** Received Data Polarity Select bit
Asynchronous mode:
1 = RX data is inverted
0 = RX data received is not inverted
Synchronous modes:
1 = Received Data (DT) is inverted. Idle state is a low level.
0 = No inversion of Data (DT). Idle state is a high level.

bit 4 **TXCKP:** Clock and Data Polarity Select bit
Asynchronous mode:
1 = TX data is inverted
0 = TX data is not inverted
Synchronous modes:
1 = Clock (CK) is inverted. Idle state is a high level.
0 = No inversion of Clock (CK). Idle state is a low level.

bit 3 **BRG16:** 16-Bit Baud Rate Register Enable bit
1 = 16-bit Baud Rate Generator – SPBRGH and SPBRG
0 = 8-bit Baud Rate Generator – SPBRG only (Compatible mode), SPBRGH value ignored

bit 2 **Unimplemented:** Read as '0'

bit 1 **WUE:** Wake-up Enable bit
Asynchronous mode:
1 = EUSART will continue to sample the RX pin – interrupt generated on falling edge; bit cleared in hardware on following rising edge
0 = RX pin not monitored or rising edge detected
Synchronous mode:
Unused in this mode.

bit 0 **ABDEN:** Auto-Baud Detect Enable bit
Asynchronous mode:
1 = Enable baud rate measurement on the next character. Requires reception of a Sync field (55h); cleared in hardware upon completion.
0 = Baud rate measurement disabled or completed
Synchronous mode:
Unused in this mode.