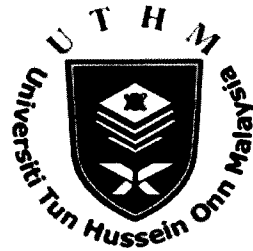


**CONFIDENTIAL**



**UNIVERSITI TUN HUSSEIN ONN MALAYSIA**

**FINAL EXAMINATION  
SEMESTER II  
SESSION 2011/2012**

**COURSE NAME** : LOGIC SYSTEM  
**COURSE CODE** : DAE 21603 / DEE 2223  
**PROGRAMME** : 2 DAE / 2 DAL / 2 DEE  
**EXAMINATION DATE** : MARCH 2012  
**DURATION** : 2 ½ HOURS  
**INSTRUCTIONS** : ANSWER FIVE (5) QUESTIONS ONLY

THIS QUESTION PAPER CONSISTS OF TEN (10) PAGES

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- Q1** (a) When the SET and RESET inputs are both high; it is usually referred to as *invalid*.
- (i) Explain why it is *invalid*.
  - (ii) Name the logic gates used for this type of latch.
- (3 marks)
- (b) For an active-LOW S-R latch, draw the logic symbol and the truth table.
- (4 marks)
- (c) Explain the difference between the operation of a gated S-R latch and an S-R flip flop.
- (4 marks)
- (d) For a D flip-flop in Figure Q1(d);
- (i) Draw the output waveform Q, relative to the input. (Note: Draw the output waveform in space provided in Figure Q1(d)(i)).
  - (ii) What specific function does this device perform?
- (4 marks)
- (e) Draw the output waveform Q, if the input signal as in Figure Q1(e) is applied to a negative edge-triggered J-K flip-flop. Assume that Q is initially LOW.
- (5 marks)
- Q2** (a) With the 555 Timer IC and RC component, draw the complete schematic diagram for the operation of;
- (i) monostable (one-shot)
  - (ii) astable multivibrator.
- (8 marks)
- (b) Determine the time width ( $t_w$ ) for monostable (One-Shot) if given  $E = 9\text{ V}$ ,  $R = 9\text{ k}\Omega$  and  $C = 10\text{ nF}$ .
- (3 marks)
- (c) Determine the value of external resistor for a 555 Timer used as an astable multivibrator with output frequency of 10 kHz,  $C = 0.001\ \mu\text{ F}$  and duty cycle of 75%.
- (9 marks)

- Q3** (a) A BCD decade counter is shown in Figure Q3(a)(i). The waveforms (Figure Q3(a)(ii)) are applied to the clock and clear input as indicated. Determine the waveforms for each of the counter output ( $Q_0$ ,  $Q_1$ ,  $Q_2$ , and  $Q_3$ ). The clear is synchronous, and the counter is started at the binary 1000 state. (Note: Draw the output waveform in space provided in Figure Q3(a)(ii)).
- (10 marks)
- (b) A 4-bit ripple counter consists of flip-flop that each has a propagation delay from clock to Q output of 12ns. How long it takes for the counter to recycle from 1010 to 1011?
- (2 marks)
- (c) How many state does a modulus-12 counter have? What is the minimum number of flip-flops required?
- (2 marks)
- (d) Draw logic diagrams to compare asynchronous counter with synchronous counter. Use at least two flip-flops for each diagram.
- (6 marks)
- Q4** The state diagram of a synchronous sequential circuit is shown in Figure Q4. Design the sequential circuit using the positive edge-triggered J-K flip-flop based on the following steps:
- (a) State table. (3 marks)
- (b) J-K flip flop excitation table. (2 marks)
- (c) J-K flip flop input equations, minimized using the Karnaugh's Map. (9 marks)
- (d) Draw the circuit implementation. (6 marks)
- Q5** (a) State two functions of a register. (2 marks)
- (b) Name four types of registers. (4 marks)

- (c) The operation of the shift register IC 74HC164 is serial in/ parallel out. The logic diagram is shown in Figure Q5(c)(i). If serial data input is fed as in Figure Q5(c)(ii), draw the expected parallel output relative to the positive edge-triggered clock.

(12 marks)

- Q6** (a) Explain the difference between *static RAM* and *dynamic RAM*.

(4 marks)

- (b) Describe the function of the following lines in a memory device.

- (i) address lines
- (ii) data lines
- (iii) chip select

(6 marks)

- (c) There are three major operations in flash memory. List all of them.

(3 marks)

- (d) What is the total bit capacity of a ROM that has 14 address lines and 8 data outputs?

(3 marks)

- (e) Explain the differences between a magneto-optical disk and a CD-ROM.

(4 marks)

- Q7** (a) Briefly explain what is a programmable logic device (PLD)

(2 marks)

- (b) Name the three (3) modes of operation for a GAL 16V8A.

(3 marks)

- (c) For the complete PLD design file as shown on Figure Q7

- (i) Draw the complete state diagram

(5 marks)

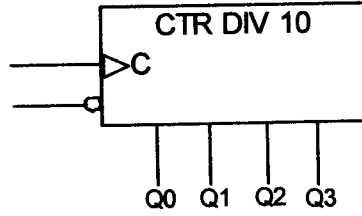
- (ii) Draw the waveform diagram. It should include the following pins CLK, QD, QC, QB, QA, GT9

(10 marks)

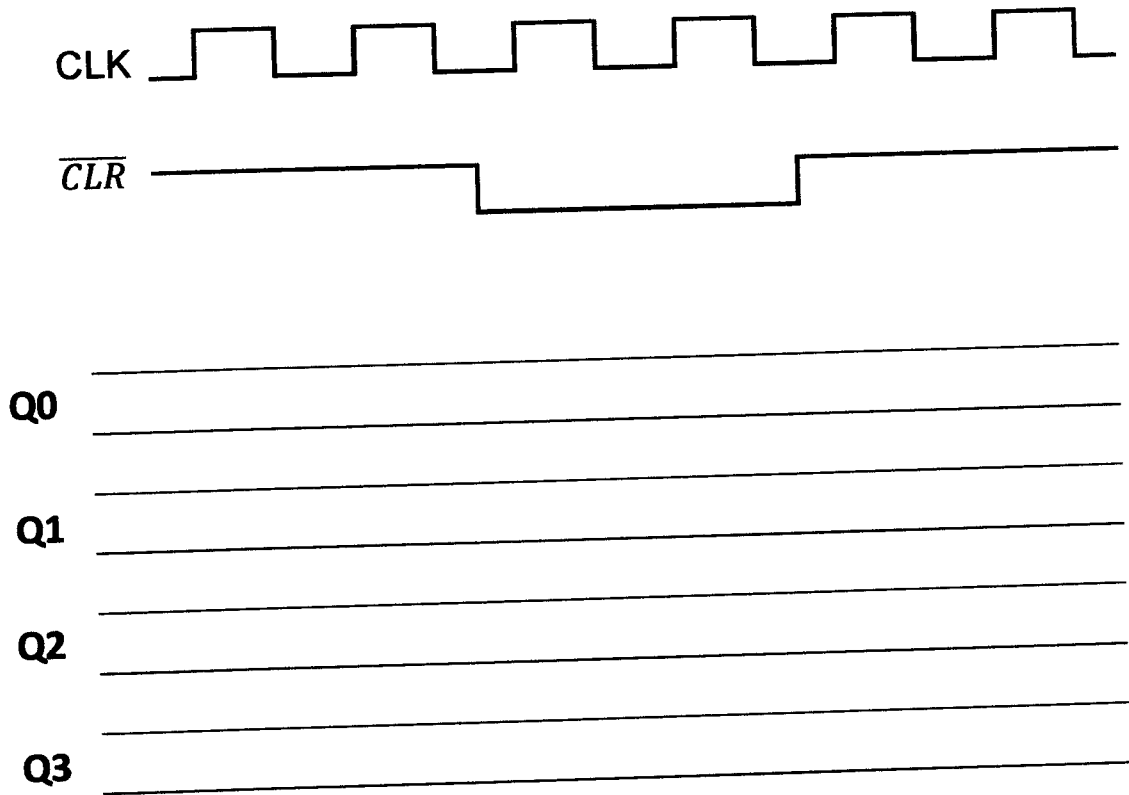
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**FIGURE Q3(a)(i)**

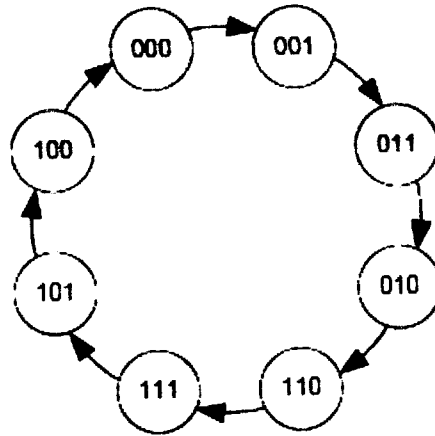


**FIGURE Q3(a)(ii)**

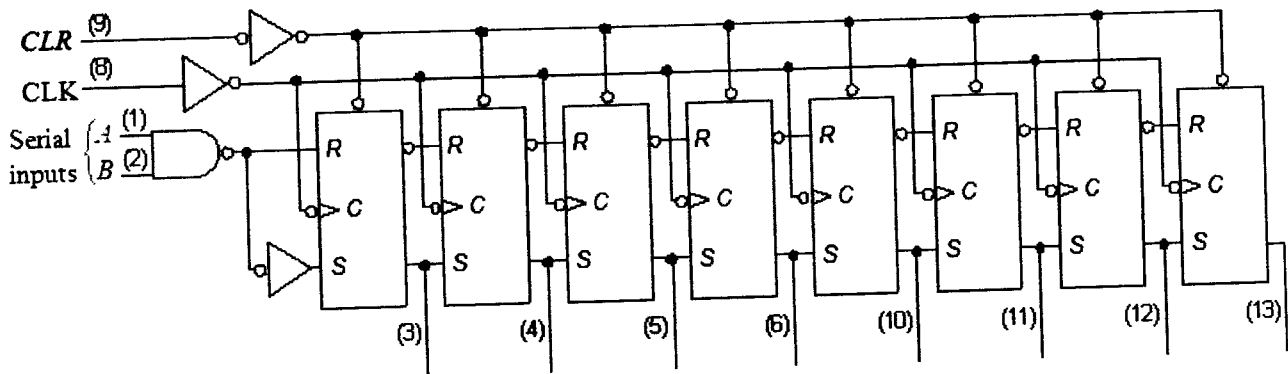
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**FIGURE 4**



**FIGURE 5(c)(i)**

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```

Name Logic Systems ;
PartNo 002 ;
Date 2/12/12 ;
Revision 01 ;
Designer Engineer B.Eng. ;
Company UTHM ;
Assembly None ;
Location Parit Raja ;
Device G16V8A ;
/* ***** INPUT PINS ***** */
PIN 1 = CLK ; /* CLOCK INPUT */
PIN 2 = !E ; /* COUNT ENABLE */
PIN 11 = !OE ; /* OUTPUT ENABLE */

/* ***** OUTPUT PINS ***** */
PIN [14..17] = [QA,QB,QC,QD] ; /* COUNTER OUTPUTS */
PIN 12 = GT9 ; /*

field COUNTER = [QD,QC,QB,QA];

$define S0 'b'0000
$define S1 'b'0001
$define S2 'b'0010
$define S3 'b'0011
$define S4 'b'0100
$define S5 'b'0101
$define S6 'b'0110
$define S7 'b'0111
$define S8 'b'1000
$define S9 'b'1001
$define S10 'b'1010
$define S11 'b'1011
$define S12 'b'1100
$define S13 'b'1101
$define S14 'b'1110
$define S15 'b'1111

sequence COUNTER {
    present S0      if E next S10;
                   default next S0;
    present S10     if E next S5;
                   default next S10;
    present S5      if E next S15;
                   default next S5;
    present S15     if E next S3;
                   default next S15;
    present S3      if E next S12;
                   default next S3;
    present S12     if E next S6;
                   default next S12;
    present S6      if E next S9;
                   default next S6;
    present S9      if E next S8;
                   default next S9;
    present S8      if E next S1;
                   default next S8;
    present S1      if E next S0;
                   default next S1;
}

GT9 = COUNTER:[10,15,12];
    
```

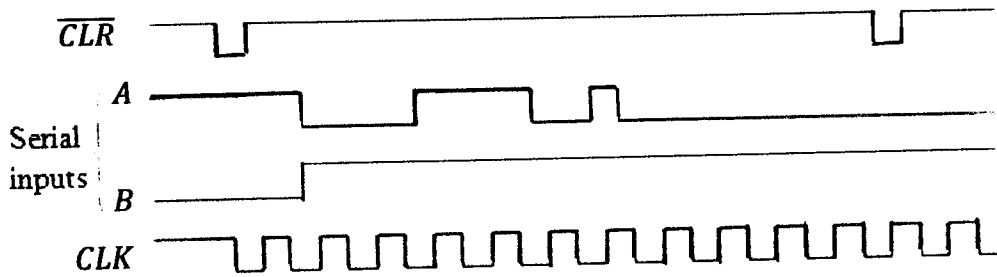
**FIGURE 7**



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Q0 \_\_\_\_\_

Q1 \_\_\_\_\_

Q2 \_\_\_\_\_

Q3 \_\_\_\_\_

Q4 \_\_\_\_\_

Q5 \_\_\_\_\_

Q6 \_\_\_\_\_

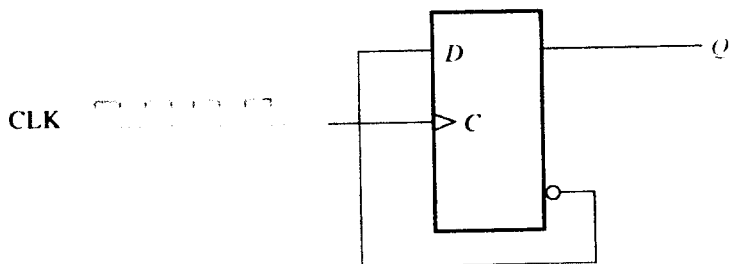
Q7 \_\_\_\_\_

**FIGURE 5(c)(ii)**

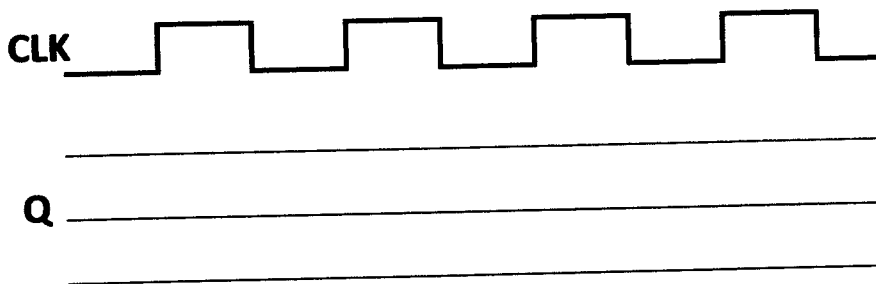
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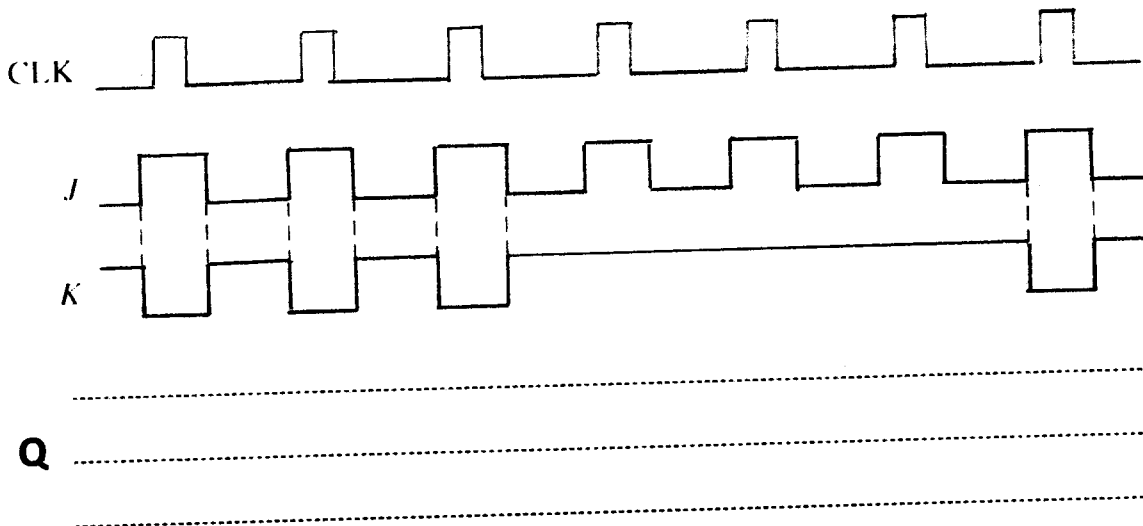
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**FIGURE Q1(d)**



**FIGURE Q1(d)(i)**



**FIGURE Q1(e)**