UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2011/2012

COURSE NAME	:	DIGITAL ELECTRONICS
COURSE CODE	:	DAE 21203 / DEE 2123
PROGRAMME	:	2 DAE/DET
EXAMINATION DATE	:	MARCH 2012
DURATION	:	2½ HOURS
INSTRUCTIONS	:	ANSWER **FOUR (4)** QUESTIONS ONLY

THIS QUESTION PAPER CONSISTS OF TEN (10) PAGES

Q1 (a) Define the following:
(i) Analog signal
(ii) Digital signal .

(4 marks)

(b) For the waveform displayed in the oscilloscope in Figure Q1(b), determine the following:
(i) The number of cycles displayed
(ii) the period, frequency and peak to peak voltage of the input signal
(iii) the duty cycle

(6 marks)

(c) A number is simply written as 1101, what is its values in decimal using bases 2, 8, 10 and 16?

(4 marks)

(d) Perform the following arithmetic operations. Show all steps.
(i) Unsigned numbers 1011110_2 divide by 4_{10}.
(ii) 37 - 28 using 2's complement
(iii) Signed numbers 1010011 + 0101010. Give answer in decimal.

(5 marks)

(e) The following is a string of ASCII characters whose bit pattern have been converted into hexadecimal for compactness:

4A 52 32 AD B5

The leftmost bit of the 8-bit in each pair of digits is the parity bit. The remaining bits are the 7-bit ASCII code.
Convert to bit form and decode them. The ASCII table is given in Table Q1(e).

(6 marks)

Q2 (a) For the logic circuit in Figure Q2(a),

(i) Write the output expression for X, Y and F.

(3 marks)

(ii) Obtain the truth table showing all inputs and outputs X, Y and F.

(5 marks)

(b) Figure Q2(b) shows the input and output patterns of a logic circuit. The inputs are ABCD and the output is W.

(i) Construct the truth table for this logic circuit.

(5 marks)

(ii) Write the output expression in sum of minterms.

(3 marks)

(iii) Simplify the output expression using k-map and implement this circuit using logic gates.

(9 marks)

Q3 (a) State 5 single variable theorems and illustrate each with basic logic gates.

(5 marks)

(b) Simplify *F* using Boolean algebra laws and DeMorgan's theorem for the following function:

$$F = \overline{\overline{A\,B}(CD + \overline{E}\,F)(\overline{A\,B} + CD)}$$

(3 marks)

(c) For the circuit in Figure Q3(c):

(i) Write the expression for output F
(ii) Implement this logic circuit using NAND gates only.

(iii) Prove that the output F for both circuit are the same.

(8 marks)

(d) Table Q3(d) shows the truth table of a combinational logic circuit.

(i) Write the output expression of the circuit in SOP form
(ii) Simplify the output expression and implement it with NOR gates only

(9 marks)

Q4 (a) Represent each function below as a sum of minterms:

i) $F(A,B,C) = AB + C$
ii) $F(X,Y,Z) = \overline{X}\,\overline{Y} + \overline{Y}Z + XY\overline{Z}$

(6 marks)

(b) Using a Karnaugh map, simplify the following equation. Obtain the minimum sum of product (SOP) expression and implement it using basic logic gates.

$$f(A,B,C,D) = \Sigma m\ (2,3,4,6,9,11,12) + d(1,14,15)$$

(8 marks)

(c) Design a 4-bit prime number detector circuit. The 4-bit input allow the binary numbers for 0 to 15 to be applied to the circuit. The output should be high only if prime numbers (1,2,3,5,7,11,13) are being input to the detector circuit.

(i) Obtain the truth table of the circuit.

(3 marks)

(ii) Simplify the output function.

(5 marks)

(iii) Implement the simplified function using basic gates.

(3 marks)

Q5 (a) Implement a full adder using two half adders:

(i) Produce a truth table

(4 marks)

(ii) Write the output expression for Sum and Carry

(3 marks)

(iii) Simplify the output expression for Sum and Carry

(4 marks)

(iv) Draw the logic circuit for the full adder.

(4 marks)

b) Figure Q5(b) shows a two 4-bit parallel binary adders with a correction circuit. Explain the operation of the adder and why the need of a correction circuit.

(10 marks)

Q6 (a) (i) What is a decoder?

(ii) How is it different from an encoder?

(4 marks)

b) Given the following function: $F = A\overline{B} + \overline{B}C + A\overline{C}$

(i) Represent F in sum of minterms. (Hint: use K-maps or truth table).

(4 marks)

(ii) Implement F using a 3 x 8 decoder with Active Low output.

(4 marks)

(iii) Implement F using a 8 x 1 multiplexer.

(3 marks)

c) The two inputs (A, B) of Figure Q6(c) are hexadecimal numbers 9_{16} (*A* input) and E_{16} (*B* input). What is the output (SUM) in binary if:

(i) $\overline{Adder / Subtractor}$ is low?

(ii) $\overline{Adder / Subtractor}$ is high?

Show all steps and give a brief explanation.

(10 marks)

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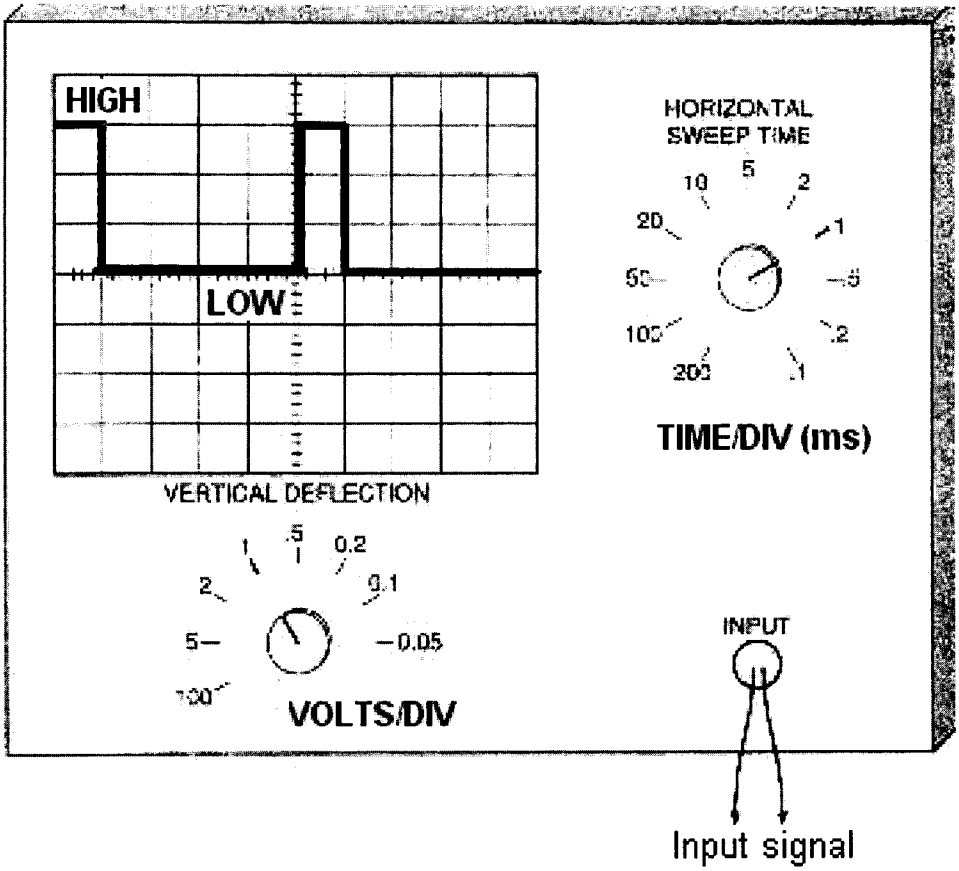

Figure Q1(b)

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Table Q1(e)

CONTROL CHARACTERS				GRAPHIC SYMBOLS											
NAME	DEC	BINARY	HEX	SYMBOL	DEC	BINARY	HEX	SYMBOL	DEC	BINARY	HEX	SYMBOL	DEC	BINARY	HEX
NUL	0	0000000	00	space	32	0100000	20	@	64	1000000	40	`	96	1100000	60
SOH	1	0000001	01	!	33	0100001	21	A	65	1000001	41	a	97	1100001	61
STX	2	0000010	02	"	34	0100010	22	B	66	1000010	42	b	98	1100010	62
ETX	3	0000011	03	#	35	0100011	23	C	67	1000011	43	c	99	1100011	63
EOT	4	0000100	04	$	36	0100100	24	D	68	1000100	44	d	100	1100100	64
ENQ	5	0000101	05	%	37	0100101	25	E	69	1000101	45	e	101	1100101	65
ACK	6	0000110	06	&	38	0100110	26	F	70	1000110	46	f	102	1100110	66
BEL	7	0000111	07	'	39	0100111	27	G	71	1000111	47	g	103	1100111	67
BS	8	0001000	08	(	40	0101000	28	H	72	1001000	48	h	104	1101000	68
HT	9	0001001	09	)	41	0101001	29	I	73	1001001	49	i	105	1101001	69
LF	10	0001010	0A	*	42	0101010	2A	J	74	1001010	4A	j	106	1101010	6A
VT	11	0001011	0B	+	43	0101011	2B	K	75	1001011	4B	k	107	1101011	6B
FF	12	0001100	0C	,	44	0101100	2C	L	76	1001100	4C	l	108	1101100	6C
CR	13	0001101	0D	–	45	0101101	2D	M	77	1001101	4D	m	109	1101101	6D
SO	14	0001110	0E	.	46	0101110	2E	N	78	1001110	4E	n	110	1101110	6E
SI	15	0001111	0F	/	47	0101111	2F	O	79	1001111	4F	o	111	1101111	6F
DLE	16	0010000	10	0	48	0110000	30	P	80	1010000	50	p	112	1110000	70
DC1	17	0010001	11	1	49	0110001	31	Q	81	1010001	51	q	113	1110001	71
DC2	18	0010010	12	2	50	0110010	32	R	82	1010010	52	r	114	1110010	72
DC3	19	0010011	13	3	51	0110011	33	S	83	1010011	53	s	115	1110011	73
DC4	20	0010100	14	4	52	0110100	34	T	84	1010100	54	t	116	1110100	74
NAK	21	0010101	15	5	53	0110101	35	U	85	1010101	55	u	117	1110101	75
SYN	22	0010110	16	6	54	0110110	36	V	86	1010110	56	v	118	1110110	76
ETB	23	0010111	17	7	55	0110111	37	W	87	1010111	57	w	119	1110111	77
CAN	24	0011000	18	8	56	0111000	38	X	88	1011000	58	x	120	1111000	78
EM	25	0011001	19	9	57	0111001	39	Y	89	1011001	59	y	121	1111001	79
SUB	26	0011010	1A	:	58	0111010	3A	Z	90	1011010	5A	z	122	1111010	7A
ESC	27	0011011	1B	;	59	0111011	3B	[	91	1011011	5B	{	123	1111011	7B
FS	28	0011100	1C	<	60	0111100	3C	\	92	1011100	5C	|	124	1111100	7C
GS	29	0011101	1D	=	61	0111101	3D	]	93	1011101	5D	}	125	1111101	7D
RS	30	0011110	1E	>	62	0111110	3E	^	94	1011110	5E	~	126	1111110	7E
US	31	0011111	1F	?	63	0111111	3F	_	95	1011111	5F	Del	127	1111111	7F

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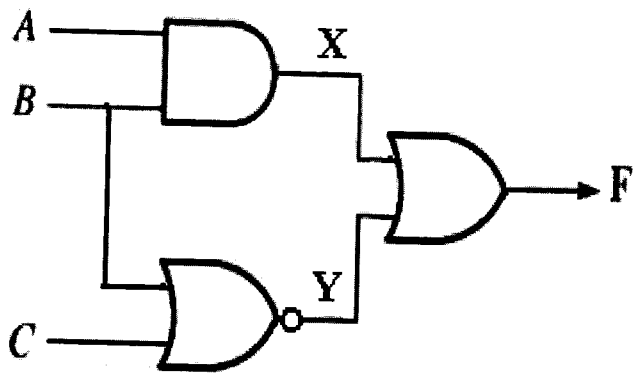

Figure Q2(a)

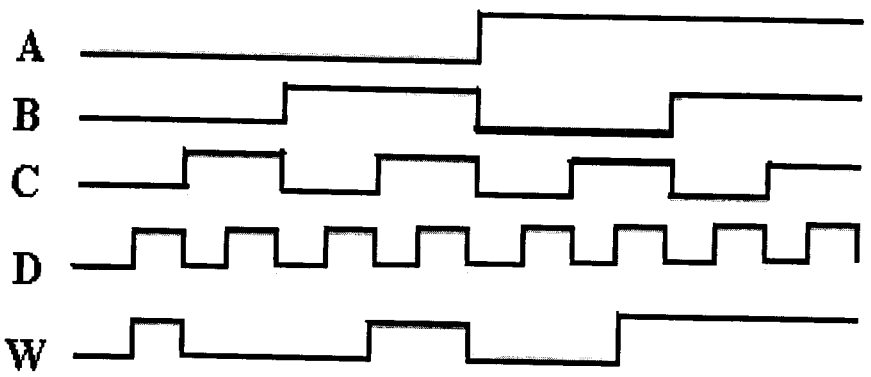

Figure Q2(b)

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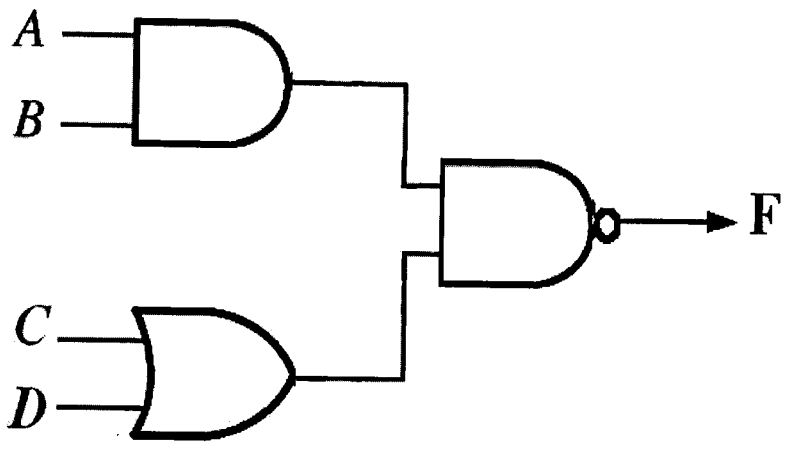

Figure Q3(c)

Table Q3(d)

INPUTS			OUTPUT
S	A	B	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

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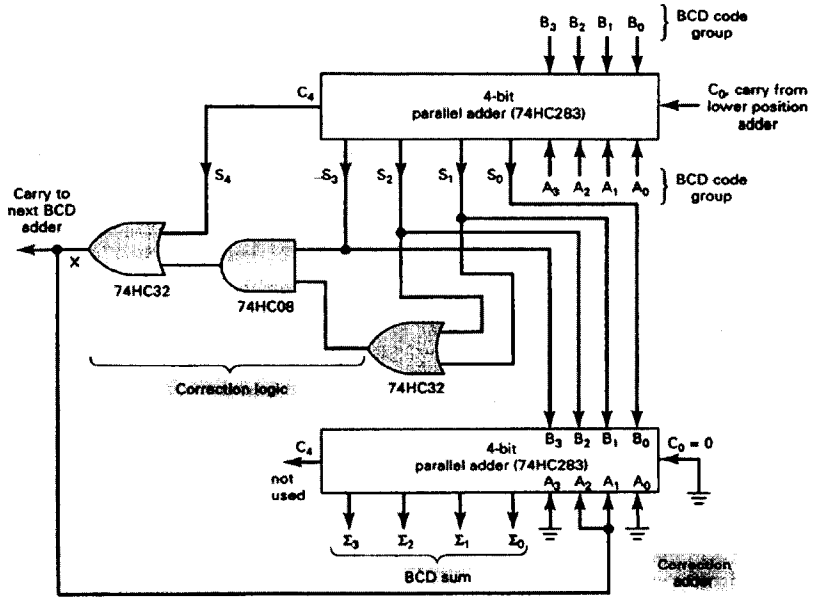

Figure Q5(b)

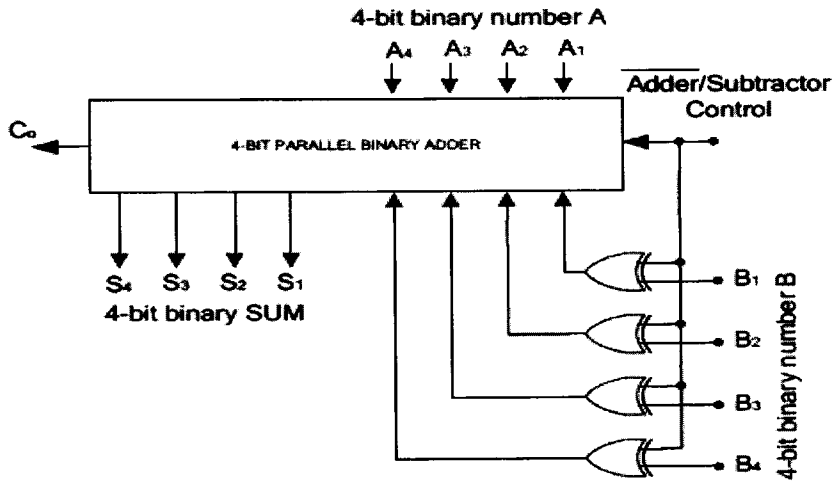

Figure Q6(c)