Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2016/2017

COURSE NAME	:	DIGITAL DEVICES AND CIRCUITS
COURSE CODE	:	BNR 23103
PROGRAMME CODE	:	BNE
EXAMINATION DATE	:	JUNE 2017
DURATION	:	3 HOURS
INSTRUCTION	:	ANSWERS **ALL** QUESTIONS

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THIS QUESTION PAPER CONSISTS OF **EIGHT (8)** PAGES

Q1 (a) State **TWO (2)** advantages of digital data as compared to analog data.

(2 marks)

(b) Find the minimal product-of-sum for the following function using K-map.

$F = \sum_{W,X,Y,Z}(0,2,3,6,8,9,12) + dontcare(1,11,13)$

(7 marks)

(c) Implement a 2-input XOR using only 2-input NAND gates. Use **FIVE (5)** or fewer NAND gates. The input are labeled A and B while the output is labeled X.

(7 marks)

(d) Contruct the truth table for the output of the circuit in **Figure Q1(d)**

(4 marks)

Q2 (a) Use only a decoder and an OR gate (of any number of inputs) create a circuit which implements the logic

$$F = (A + B)(A + \overline{C})(A + \overline{B} + C)$$

(5 marks)

(b) **Table Q2(b)** shows the truth table of a combinational logic circuit. Draw the gate using ONLY a 4:1 multiplexer and two inverters. Connect input A and B to the selection lines S1 and S0 respectively. The input requirement for the 4 data lines will be a function of the variables C and D.

(9 marks)

(c) Complete the timing diagrams for the circuits depicted in **Figure Q2(c) (i)** and **Figure Q2(c) (ii)**.

(6 marks)

Q3 (a) Explain the differences between D flip-flop and J-K flip-flop with the aid of their truth table and positive edge-triggered flip-flop logic symbols.

(4 marks)

(b) By using J-K flip-flops, design a counter to produce the following sequence of 1,4,3,5,7,6,2,1....Your design should include next-state table, transition table, K-map simplification and implementation of circuit.

(10 marks)

(c) Determine the sequence of the counter in **Figure Q3(c)**. Begin with the counter cleared.

(6 marks)

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Q4 (a) Consider a Moore finite state machine with two inputs, w and x, and a single output y.

(i) Produce a state transition table for the design illustrated in **Figure Q4(a)(i)**. Use don't care 'X' notation for other condition.

(4 marks)

(ii) How many D flip-flops are required to realize the finite state machine in (i)?

(2 marks)

(b) You are part of a team required to design a Mealy sequence detector using D flip-flop / JK flip-flop as part of a large design project. The sequence detector should assert the output, Z for one clock period, when the pattern 11011 is observed on a serial stream of data on the input, X=11011011011 where sequences can overlap. As a technologist, you are required to choose the simplest design between D flip-flop and JK flip-flop to reduce the total cost of the project.

(14 marks)

Q5 (a) An analogy for a shift register is a conveyor belt as shown in **Figure Q5(a)**. The illustration showing a single conveyor belt at four different times. State and explain which shift register operations of the following sequence represents.

(4 marks)

(b) **Figure Q5(b)(i)** shows a shift register circuit energizes one LED at a time (beginning with the bottom LED at power-up), in a rotating pattern that moves at the pace of the clock. A technician decides to reverse the direction of pattern motion, and alters the circuit as shown in **Figure Q5(b)(ii).** Unfortunately, this does not work as planned. Now, the bottom LED blinks once upon power-up, then all LEDs remain off. As a technologist, you are required to find and solve the problem made by the technician.

(6 marks)

(c) Design a 4-bit shift register with parallel load using D flip-flops. There are two control inputs: shift and load. When shift = 1, the content of the register is shifted by one position. New data is transferred into the register when load = 1 and shift = 0. If both control inputs are equal to 0, the content of the register does not change.

(10 marks)

- END OF QUESTIONS -

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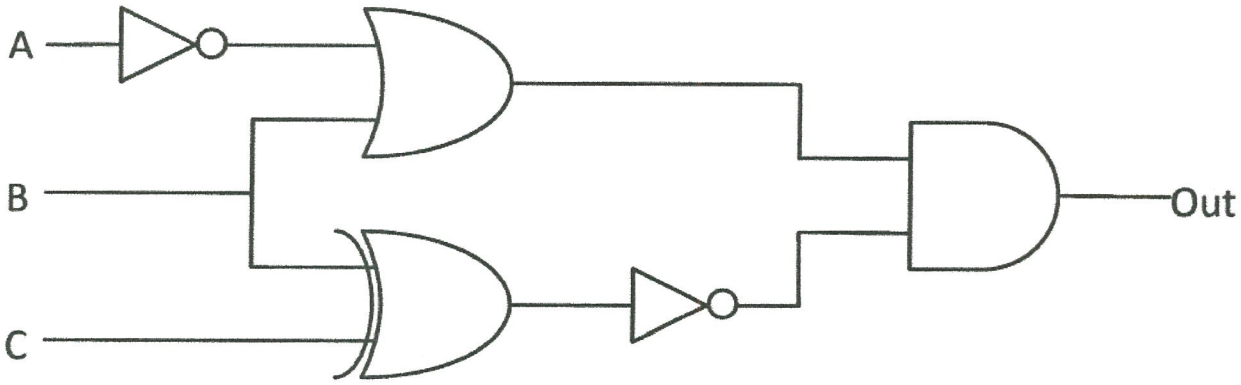

FIGURE Q1(d)

TABLE Q2(b)

A	B	C	D	F
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

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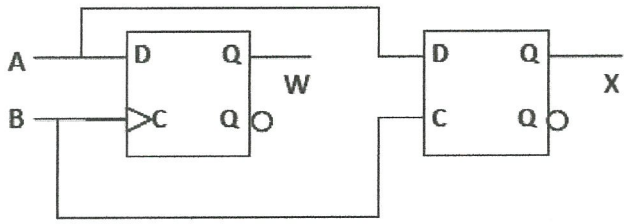


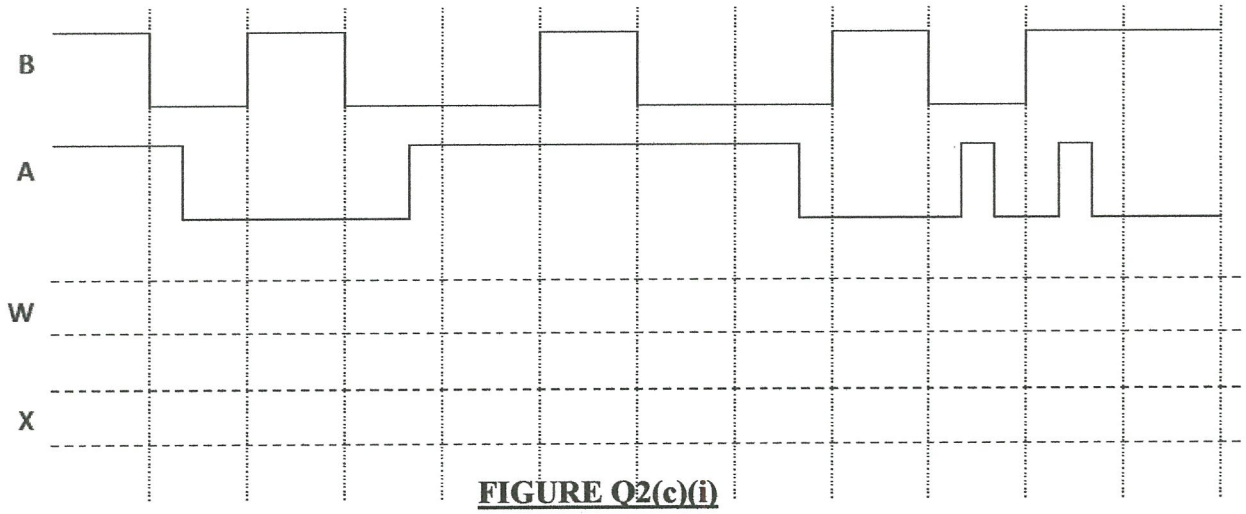
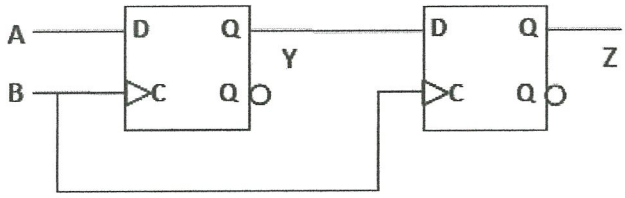


FIGURE Q2(c)(i)



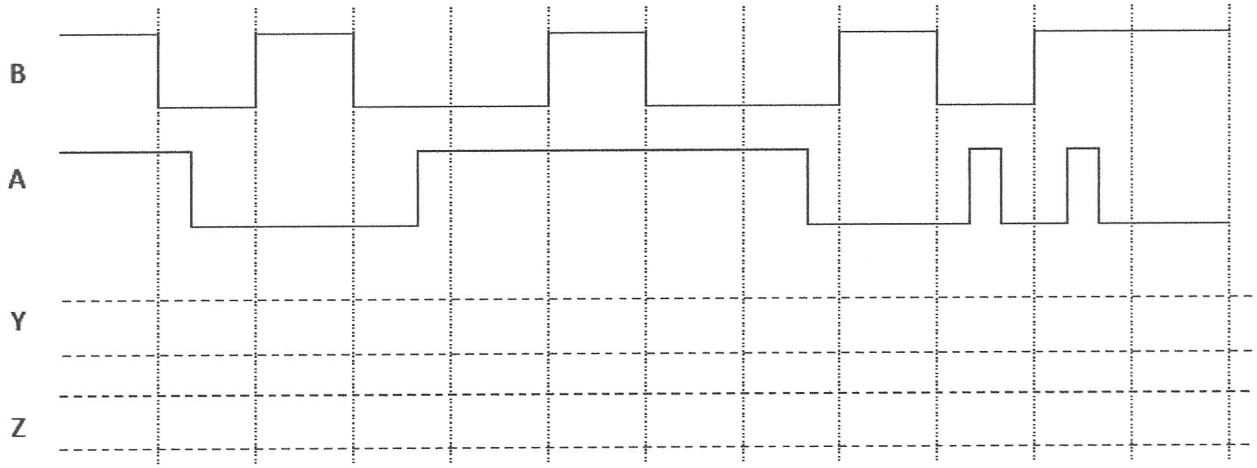


FIGURE Q2(c)(ii)

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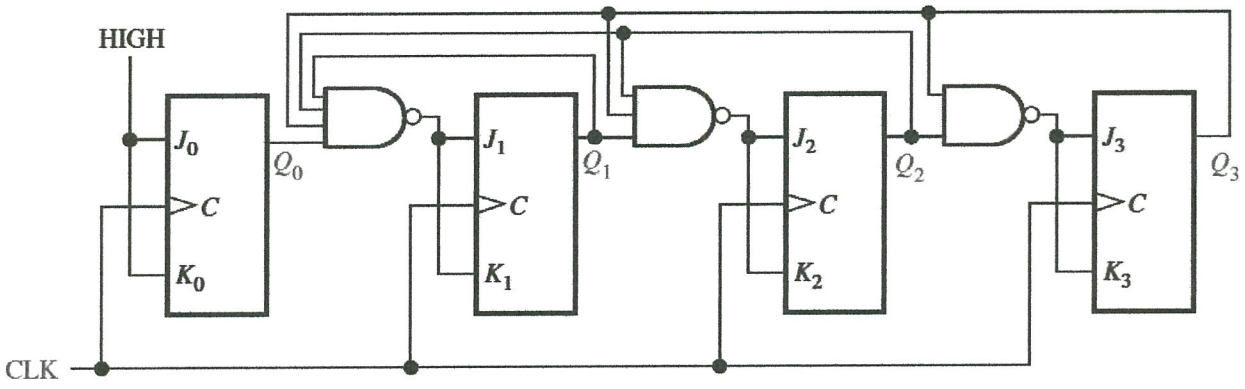

FIGURE Q3(c)

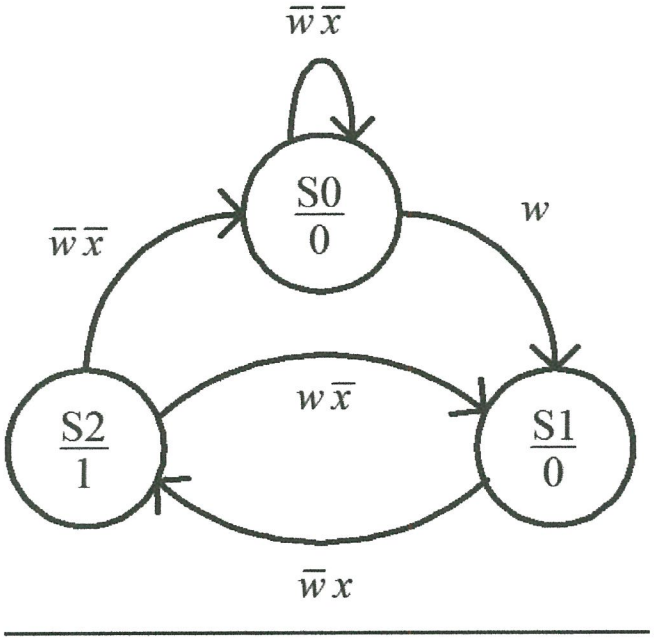

FIGURE Q4(a)(i)

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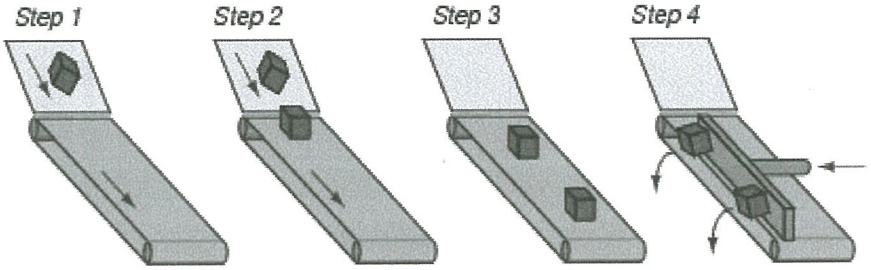
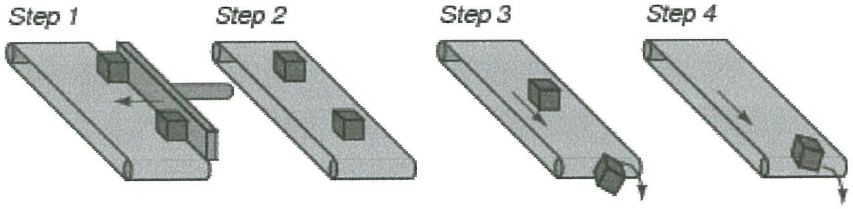


(i)



(ii)

FIGURE Q5(a)

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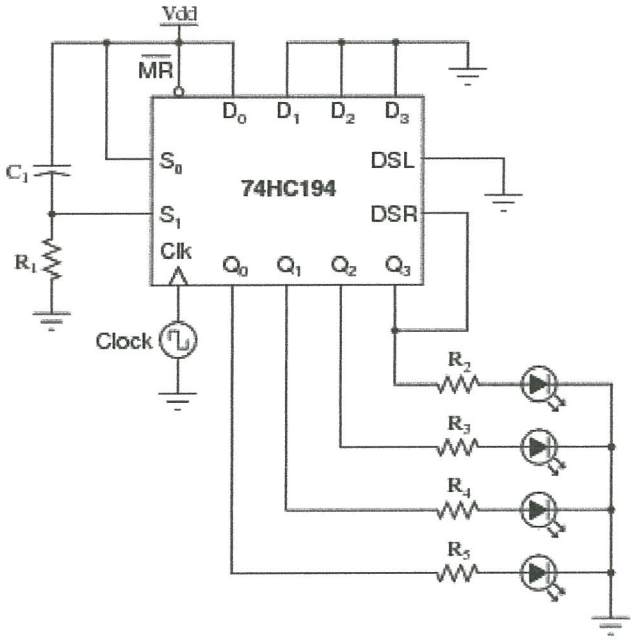
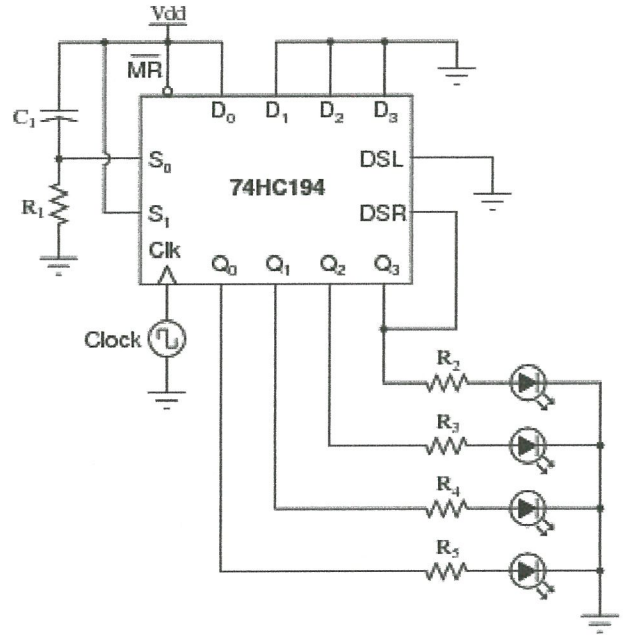


(i)



(ii)

FIGURE Q5(b)

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