Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2016/2017

COURSE NAME	:	ELECTRONIC DEVICES AND CIRCUITS I
COURSE CODE	:	BNR25803
PROGRAMME CODE	:	BNE
EXAMINATION DATE	:	DECEMBER 2016 / JANUARY 2017
DURATION	:	2 HOURS 30 MINUTES
INSTRUCTION	:	ANSWERS **FOUR (4)** QUESTIONS ONLY

THIS QUESTION PAPER CONSISTS OF **NINE (9)** PAGES

Q1 (a) Describe briefly on the following diode circuits:

(i) Clipper

(2 marks)

(ii) Clamper

(2 marks)

(b) Determine the currents I_1, I_2 and I_{D2} for the network of **Figure Q1 (b)**.

(5 marks)

(c) Plot the output voltage, $V_o(t)$, for each of the circuits in **Figure Q1 (c)** if the input voltage is V_i.

(5 marks)

(d) In the voltage regulator circuit in **Figure Q1 (d)**, let $V_i = 6.3$V, $R = 12\Omega$, and $V_z = 4.8$V. The zener diode current is to be limited to the range $5 \leq I_z \leq 100$ mA.

(i) Determine the range of possible load currents and load resistances.

(6 marks)

(ii) Determine the power rating required for the Zener diode and the load resistor, R_L.

(5 marks)

Q2 (a) A power supply circuit is energized by a 240 V_{rms}, 50Hz AC source. The transformer step-down ratio is 16:1 and it uses a full-wave bridge rectifier with a single 1000μF electrolytic capacitor filter, C_1. Do the following:

(i) Draw the schematic diagram for this DC power supply circuit.

(3 marks)

(ii) Calculate the peak value of the ripple voltage $V_{r(p)}$ and the DC output voltage, $V_{r(dc)}$ for this power supply if the load current is 0.1 A. Assume that the forward voltage drops of each diode is 0.7 V.

(7 marks)

(iii) Sketch the output voltage, V_{out} and label the peak value and dc level.

(3 marks)

(iv) Determine the percentage of ripple factor (r %) for this the circuit.

(3 marks)

(b) In order to improve the previous ripple factor of the power supply circuit in **Q2(a)**, the output of this circuit is now connected to the LC filter circuit as shown in **Figure Q2(b)**. Calculate the new ripple factor (r %) of the output waveform. Given $C_2 = C_1$ and the inductor has winding resistance of 2Ω.

(9 marks)

Q3 (a) With the aid of appropriate diagrams, explain the following devices:

(i) Gate turn-off switch (*GTO*)

(5 marks)

(ii) Silicon controlled rectifier (*SCR*)

(5 marks)

(b) Describe two techniques for turning an *SCR* (silicon-controlled rectifier) ON and OFF.

(5 marks)

(c) For a unijunction transistor (*UJT*) with $V_{BB} = 20$ V, $\eta = 0.65$, $R_{B1} = 2$ kΩ ($I_E = 0$), and $V_D = 0.7$ V, determine:

(i) R_{B1} R_{B2}

(2 marks)

(ii) R_{BB}

(2 marks)

(iii) V_{RB1}

(2 marks)

(iv) V_P

(2 marks)

(d) Draw the UJT equivalent circuit completed with all the values to represent the UJT at part **Q3(c)**.

(2 marks)

Q4 (a) Differentiate between Bipolar Junction Transistor (*BJT*) and Field Effect Transistor (*FET*).

(4 marks)

(b) Explain with a suitable diagram, **THREE (3)** operating region of a BJT.

(6 marks)

(c) Prove that the relationship between current gain of a BJT, α and β are as shown below if $\alpha = I_C/I_E$ and $\beta = I_C/I_B$.

$$\alpha = \frac{\beta}{\beta + 1} \quad \text{or} \quad \beta = \frac{\alpha}{1 - \alpha}$$

(5 marks)

(d) An n-channel enhancement-type MOSFET (*E-MOSFET*) has following parameters; $V_{GS(on)} = 4$ V, $I_{D(on)} = 3$ mA, $k = 0.4 \times 10^{-3}$ A/V^2.

(i) Determine the threshold voltage, $V_{GS(TH)}$ and write the general expression for I_D.

(3 marks)

(ii) Sketch and completely label the transfer characteristics for this E-MOSFET.

(3 marks)

(iii) Determine I_D for $V_{GS} = 3$V, 6V and 10V.

(4 marks)

Q5 (a) Draw the BJT logic gates that represents *OR* and *AND* gate. Give the truth table for both gates.

(6 marks)

(b) For a bipolar transistor constant current source as shown in **Figure Q5(b)**, calculate the constant current, *I*.

(5 marks)

(c) For the transistor voltage regulator circuit shown in **Figure Q5(c)**, calculate the output voltage, V_o and zener current, I_Z for $R_L = 1$ kΩ. The transistor has $\beta = 50$.

(7 marks)

(d) Give the differences between Class A, Class B, Class AB and Class C power amplifier. Identify the major problem occurs in Class B power amplifier compared to other classess. Discuss your answer.

(7 marks)

Q6 (a) Differentiate between negative feedback and positive feedback.

(4 marks)

(b) **Figure Q6 (b)** is a block diagram of a system with feedback network. Derive the closed-loop gain, A_f of the system.

(6 marks)

(c) **Figure Q6 (c)** shows an amplifier with a negative feedback network. Given Z_{of} = 100 kΩ, Z_o = 5 kΩ and A_f = 50.

(i) State the feedback topology and the amplifier type.

(2 marks)

(ii) Calculate the gain without feedback, A and the feedback factor, β.

(6 marks)

(iii) If the low cutoff frequency of the amplifier with feedback network (f_{Lf}) is 100 Hz, calculate the low cutoff frequency (f_L) if the amplifier does not have the feedback network.

(3 marks)

(iv) Sketch and label the values of the frequency response for both conditions, with and without feedback.

(4 marks)

- END OF QUESTION -

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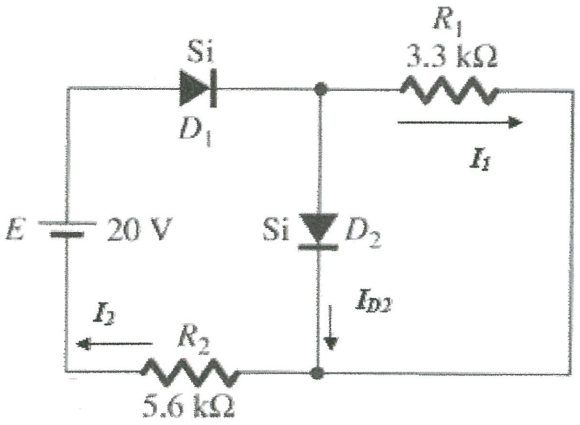

FIGURE Q1 (b)

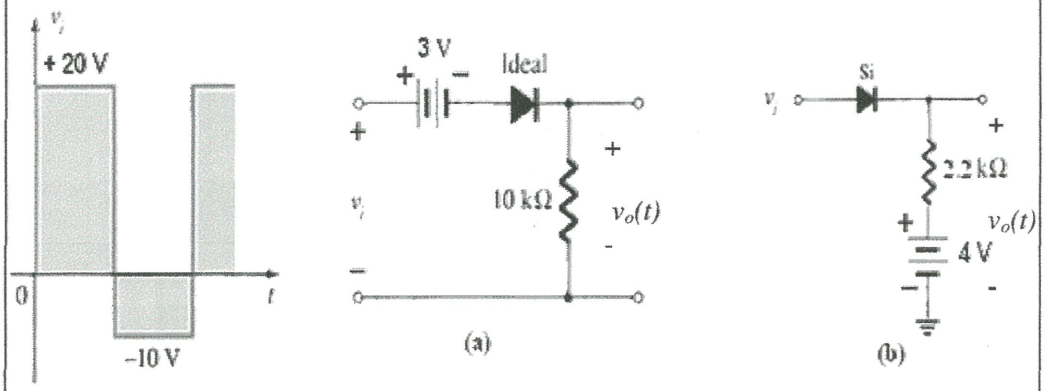

FIGURE Q1 (c)

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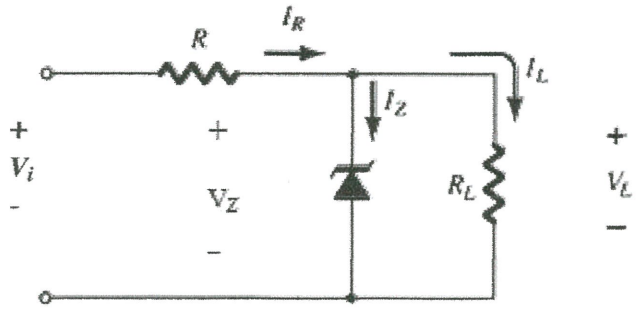

FIGURE Q1(d)

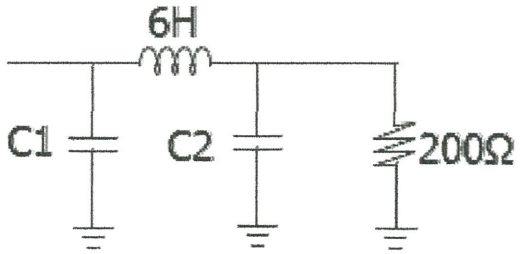

FIGURE Q2 (b)

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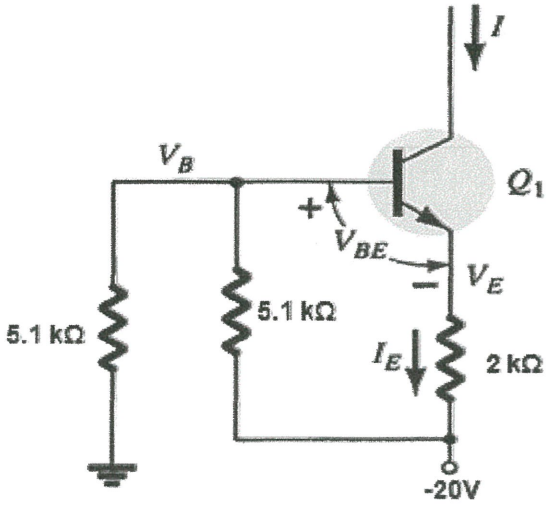

FIGURE Q5(b)

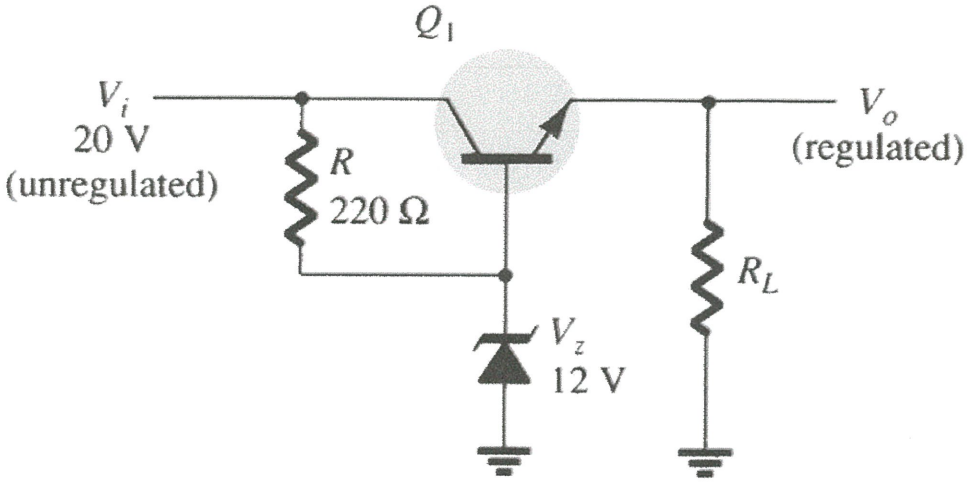

FIGURE Q5(c)

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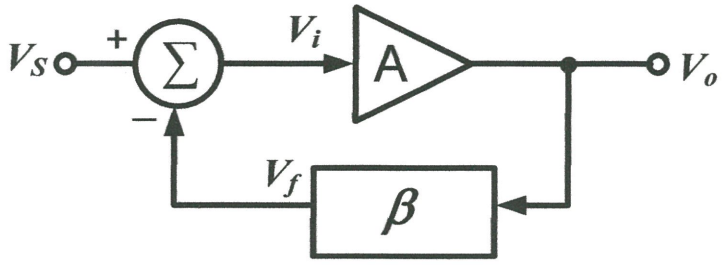

FIGURE Q6 (b)

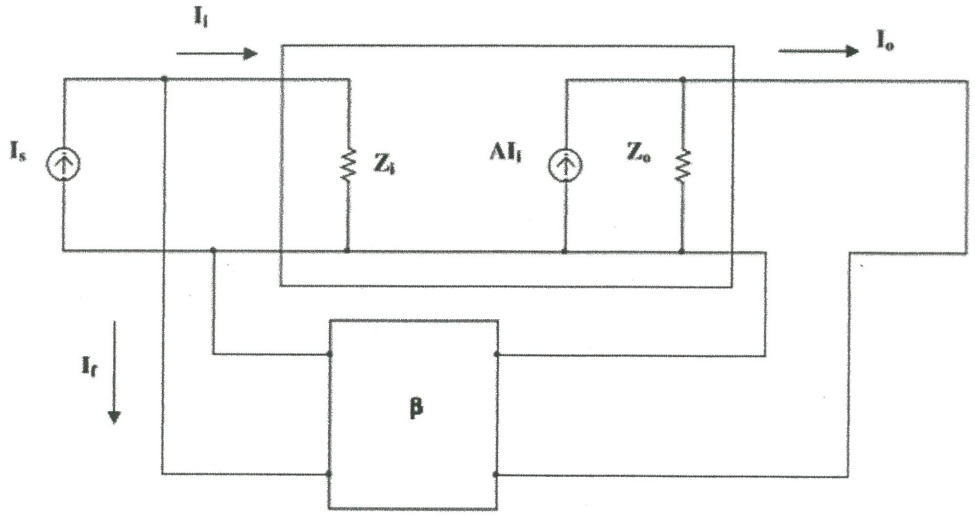

FIGURE Q6 (c)