Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2016/2017

COURSE NAME	:	DIGITAL ELECTRONICS
COURSE CODE	:	BNR 25402
PROGRAMME CODE	:	BND / BNF
EXAMINATION DATE	:	DECEMBER 2016 / JANUARY 2017
DURATION	:	2 HOURS 30 MINUTES
INSTRUCTION	:	ANSWER **FOUR (4)** QUESTIONS ONLY

THIS QUESTION PAPER CONSISTS OF **NINE (9)** PAGES

Q1 (a) Convert the binary number 101011011_2 to:

(i) octal (1 mark)

(ii) hexadecimal (1 mark)

(iii) decimal (1 mark)

(iv) BCD (1 mark)

(b) Perform the following arithmetic operations. Show all steps.

(i) 58 - 63 using 2's complement. (2 marks)

(ii) $A1_{hex} - 72_{hex}$ using 2's complement. (2 marks)

(c) Write the next four numbers in this hexadecimal counting sequence:
8FD, 8FE, _____, _____, _____, _____. (2 marks)

(d) Use Karnaugh map to simplify the following function.

$$f(A,B,C,D) = \Sigma(0,1,3,5,14,15) + d(4,7,11,13)$$

(5 marks)

(e) (i) Simplify the following Boolean expression using Boolean algebra and verify the result using a Karnaugh map:

$$\mathbf{F = XY\bar{Z} + XY + X\bar{Y}Z}$$

(6 marks)

(ii) Implement the simplified expression using NAND gates only. (4 marks)

Q2 (a) For the circuit in **Figure Q2(a)**,

(i) Write the Boolean Expression for outputs X, Y and Z. (3 marks)

(ii) Obtain the truth table showing all inputs and outputs. (4 marks)

(b) Waveforms A, B and C of **Figure Q2(b)** are applied to a logic circuit. The output waveform, F is as shown in **Figure Q2(b)**.

(i) Obtain the truth table.

(2 marks)

(ii) Write the logic expression for F.

(2 marks)

(iii) Draw the logic circuit for function F.

(2 marks)

(c) From the truth table in **Table Q2(c)**.

(i) Write the standard sum of product (SOP) expression for output F.

(2 marks)

(ii) Write the standard product of sum (POS) expression for F

(2 marks)

(iii) Use the K map to get the minimum sum of product (SOP) expression for F.

(4 marks)

(iv) Implement the simplified expression of F with NAND gates only.

(4 marks)

Q3 (a) Build the truth table of a half-adder circuit showing all inputs and outputs (SUM and carry (C_O). Write the expression for both outputs.

(7 marks)

(b) The following is the output expression for a Full Adder circuit. Illustrate how a full-adder can be implemented using 2 half-adders.

$$SUM = A \oplus B \oplus C_{in}$$

$$C_O = C_{in}(A \oplus B) + AB$$

(6 marks)

(c) Build the truth table for a full adder circuit showing all inputs and outputs (SUM and carry (C_O)).

(i) Write the expression for both outputs in sum of minterms form.

(7 marks)

(ii) Implement the full adder circuit using the 74138 IC shown in **Figure Q3(c)**. Label all inputs and outputs.

(5 marks)

Q4 (a) With the aid of truth tables, describe the differences between the following flip flops:

(i) RS flip flop

(3 marks)

(ii) JK flip flop

(2 marks)

(iii) D fip flop

(2 marks)

(b) **Figure Q4(b)** shows a 7476 JK flip-flop and timing diagram showing 3 inputs: clock input (CLK), J and K. Assume that the two asynchronous inputs CLEAR and PRESET is high. Q is initially LOW. Draw the Q output waveform.

(6 marks)

(c) **Figure Q4(c)(i)** shows two flip flops connected together.

(i) Sketch the output waveform for Q_0 and Q_1 in **Figure Q3(c)(ii).**

(5 marks)

(ii) Determine the output frequency at Q_1 if the input frequency (CLK) is 2 kHz.

(3 marks)

(iii) Explain its operation

(4 marks)

Q5 (a) With the aid of diagrams, describe the following devices:

(i) A decoder
(ii) A multiplexer

(6 marks)

(b) Given the following function: $F = \overline{X}\overline{Y} + \overline{Y}Z + XY\overline{Z}$

(i) Represent F in sum of minterms. (Hint: use K-maps or truth table).

(4 marks)

(ii) Implement F using the 3 x 8 decoder.

(3 marks)

(iii) Implement F using a 8 x 1 multiplexer.

(3 marks)

(c) State **TWO (2)** differences between synchronous and asynchronous counters.

(4 marks)

(d) Design a MOD 8 asynchronous counter using JK flip-flops.

(i) Draw the circuit.

(2½ marks)

(ii) Determine the counting sequence.

(2½ marks)

Q6 (a) The 4-bit serial input register in **Figure Q6(a)** has 1011 (Q,R,S,T) stored in it and data inputs are low. Show the register operations for four clock transitions by doing the following:

(i) Draw a table showing the state sequence

(5 marks)

(ii) Draw the timing diagram.

(5 marks)

(b) Briefly explain **TWO (2)** advantages of digital techniques over analog. Give **ONE (1)** major drawback of digital techniques.

(4 marks)

(c) Two conversion are necessary to interface real world, analog signals with a digital circuit. Name and describe briefly the function of the two circuits used.

(3 marks)

(d) The circuit in **Figure Q6(d)(i)** is used in digital and analog interface.

(i) State the function of this circuit.

(ii) Determine the output V_{out} and record its value in **Table Q6(d)** if the 4-bit numbers D_3, D_2, D_1 and D_0 are applied to the inputs.

(8 marks)

- END OF QUESTIONS –

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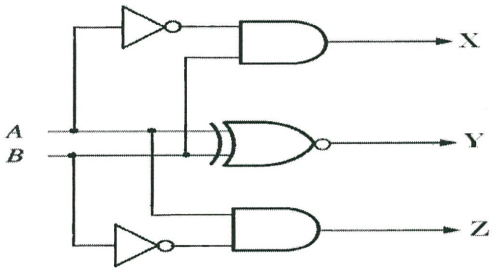

Figure Q2(a)

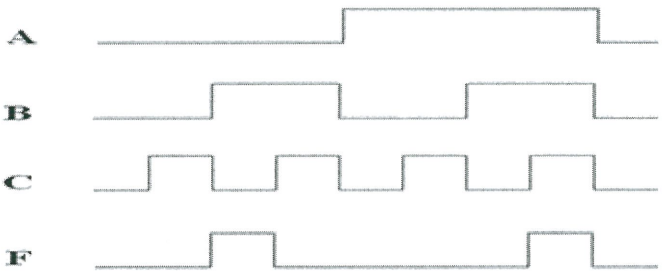

Figure Q2(b)

TABLE Q2(c)

INPUT			OUTPUT
X	Y	Z	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

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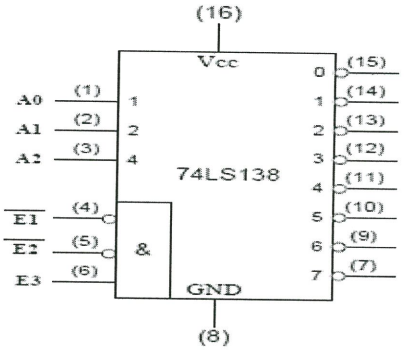

Figure Q3(c)

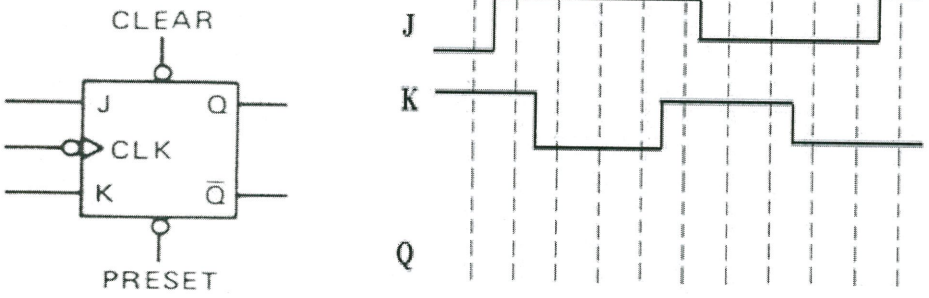

Figure Q4(b)

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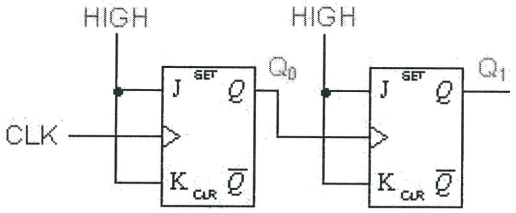

Figure Q4(c)(i)

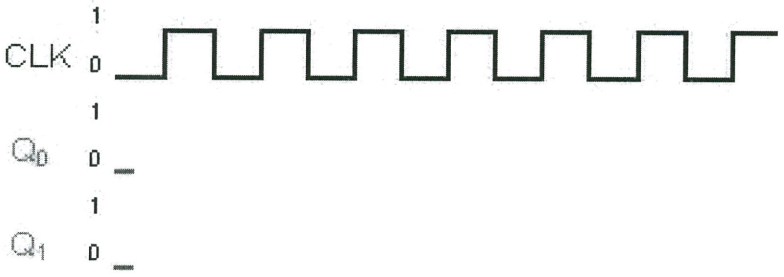

Figure Q4(c)(ii)

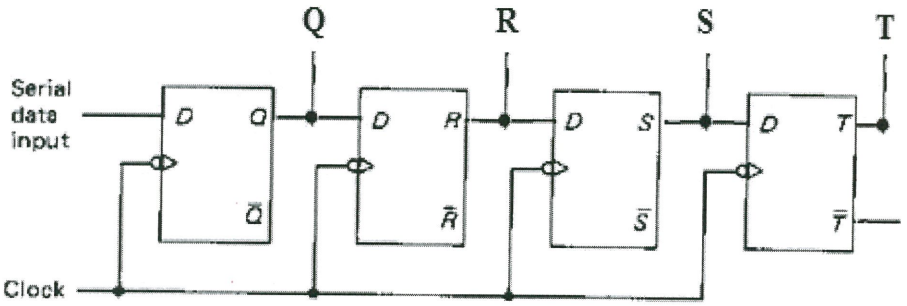

Figure Q6(a)

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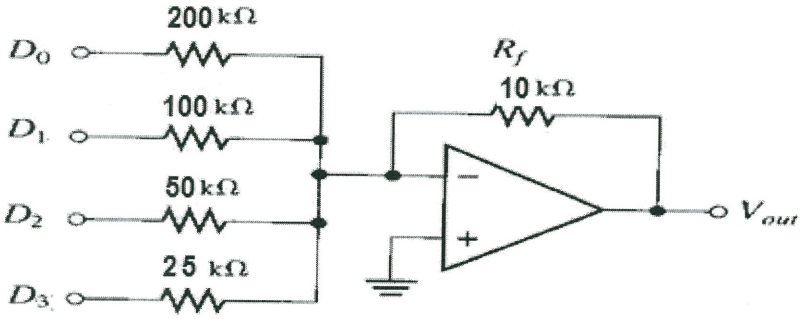

Figure Q6(d)(i)

Table Q6(d)

D_3	D_2	D_1	D_0	V_{out} (V)
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	