UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2014/2015

COURSE NAME	:	ELECTRONIC CONTROL TECHNOLOGY
COURSE CODE	:	BNR23003
PROGRAMME	:	2 BNE
EXAMINATION DATE	:	JUNE/JULY 2015
DURATION	:	3 HOURS
INSTRUCTION	:	ANSWER **FIVE (5)** QUESTIONS ONLY

THIS QUESTION PAPER CONSISTS OF **TEN (10)** PAGES

Q1 (a) Explain two types of Industrial Control Classification and give an example for each class.

(5 marks)

(b) Figure Q1(b) shows the Closed Loop Antenna system. From this figure:

(i) Draw the equivalent block diagram for the system

(ii) Analysed what will be the error signal and antenna movement when the azimuth angle output:

- equal to the desired azimuth angle input,
- less than the desired azimuth angle input
- greater than the desired azimuth angle input.

(9 marks)

(c) When a computer is used in digital control system, debate why it is not possible to maintain the analog relationships ?

(6 marks)

Q2 (a) Explain how Schmitt Trigger function and how it utilizes the *hysteresis* effect.

(4 marks)

(b) Figure Q2(b) shows the Schmitt Trigger input signal with the positive going threshold 1.7V and negative going threshold 0.9V. Based on the input signal in Figure Q2(b),

(i) Construct the Schmitt Trigger output.

(ii) Explain the process of getting the output from Schmitt Trigger input.

(11 marks)

(c) (i) Figure Q2(c)(i) shows one of the signal processor device. What is the name of the device? If the input signal is a quare wave, what will be the output signal?

(ii) Figure Q2(c)(ii) also shows one of the signal processor device. What is the name of the device? If the input signal is a triangular wave, what will be the output signal?

(5 marks)

Q3 (a) Figure Q3(a) shows the summing amplifier. If $R_1 = 40k\Omega$, $R_2 = 10\ k\Omega$, $R_3 = 15\ k\Omega$ and $R_F = 15\ k\Omega$, calculate

(i) Current flow through R_1, R_2, R_3 and R_F,

(ii) V_{out}.

(9 marks)

(b) Figure Q3(b) shows the digital to analog converter (DAC).

(i) Calculate the analog output voltage (Vout) if a binary 1101 is applied.

(ii) Find the resolution of the DAC.

(11 marks)

Q4 (a) Figure Q4(a) shows a logic circuit consist of OR, AND and NOT gate.

(i) By analysing the logic circuit using truth table, identify what is the equivalent logic function that the Figure Q4(a) represent ?

(ii) Using the logic circuit in Figure Q4(a), construct the ladder diagram.

(9 marks)

(b) Figure Q4(b) shows the overload protection circuit.

(i) By analysing Figure Q4(b), develop the ladder diagram for the whole circuit.

(ii) Using the ladder diagram developed in Q4(b)(i), explain how the overload protection circuit work.

(11 marks)

Q5 (a) Explain the concept of PLC development.

(2 marks)

(b) List 4 function in PLC and explain the role of each function.

(4 marks)

(c) Figure Q5(c) shows the block diagram of PLC input interface circuit.

(i) What happen if "detection and conditioning circuit" is not function ?

(ii) What happen if the "threshold circuit" is faulty?

(6 marks)

(d) Figure Q5(d) shows the ladder diagram for Omron CQM1H PLC using ON-delay type timer. The timing setting is from 0000 - 9999 that is equivalent to 000.0 sec - 999.9 sec respectively. From Figure Q5(d), write the mnemonics of the ladder diagram.

(8 marks)

Q6 Figure Q6 shows the "Conveyor/Inspection System" using a shift register. Figure (a) show the physical layout of the system. Figure (b) shows the control circuit of the system, illustrating the use of a shift register to keep track of the progress of parts through the system. The conveyor systems were divided into 4 zones, where each flip-flop in the shift register represents one zone on the conveyor system. The system are setting to determine either the part passes inspection and is routed to the next production location or it fails inspection and is rejected. When reaching zone 4, good part will continue to the next zone while bad part will dumped into the reject bin.
Explain clearly how this "Conveyor/Inspection System" using a shift register to isolate the good and bad parts.

(20 marks)

- END OF QUESTION –

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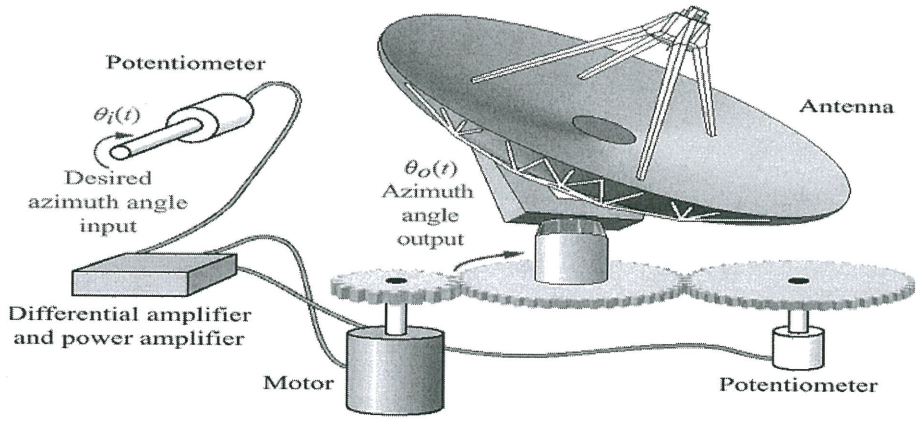

FIGURE Q1(b)

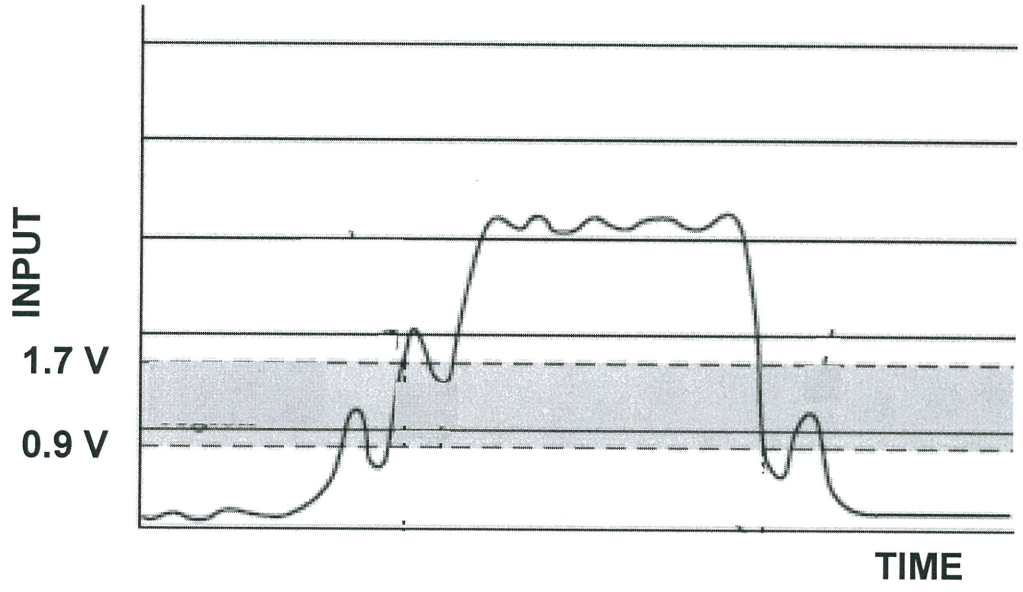

FIGURE Q2(b)

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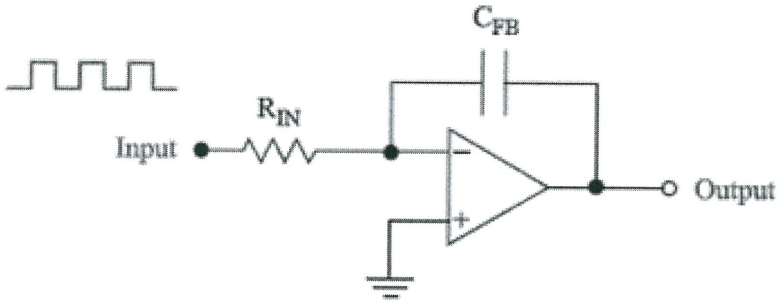

FIGURE Q2(c)(i)

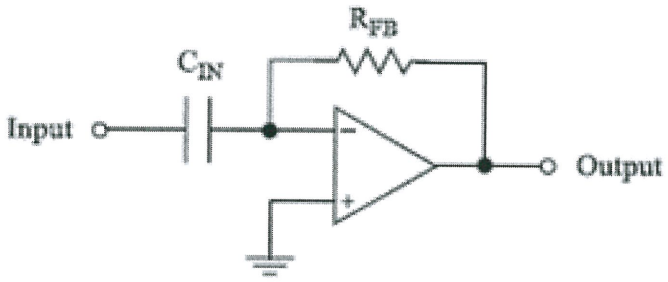

FIGURE Q2(c)(ii)

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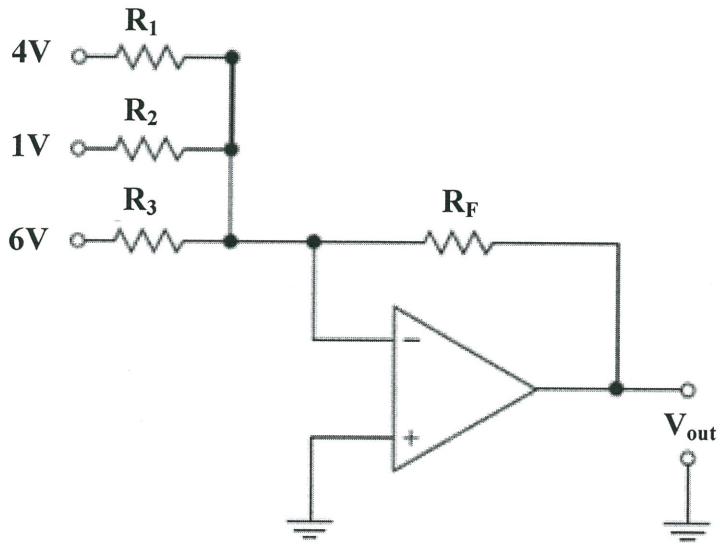

FIGURE Q3(a)

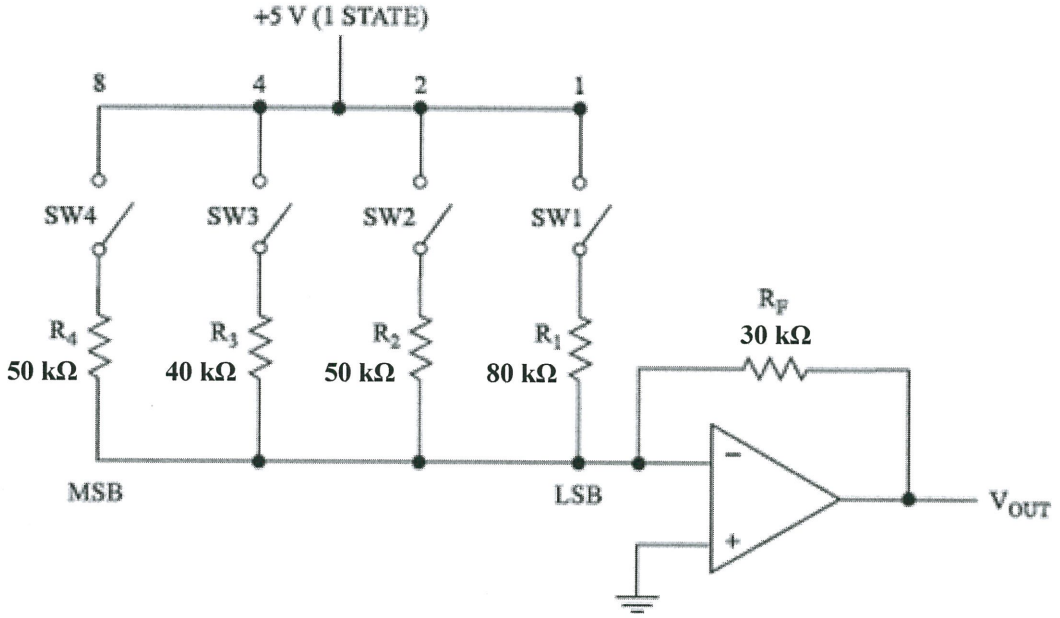

FIGURE Q3(b)

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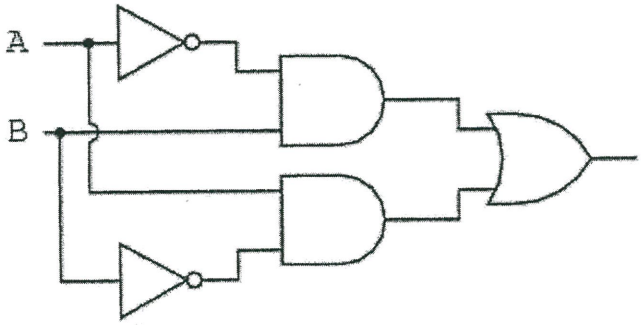

FIGURE Q4(a)

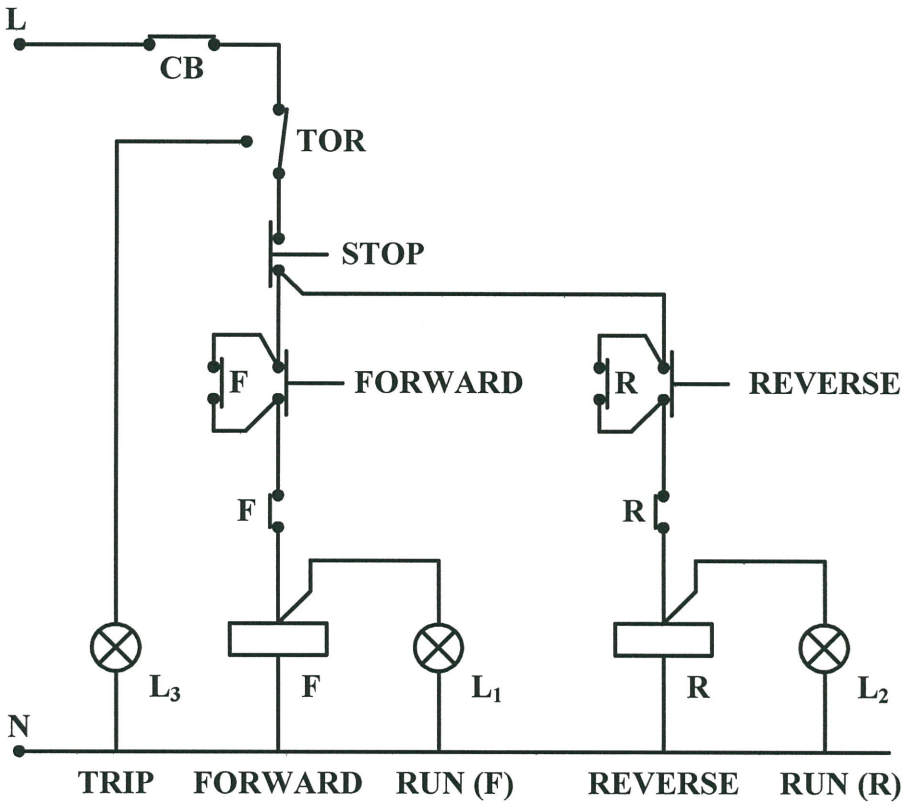

FIGURE Q4(b)

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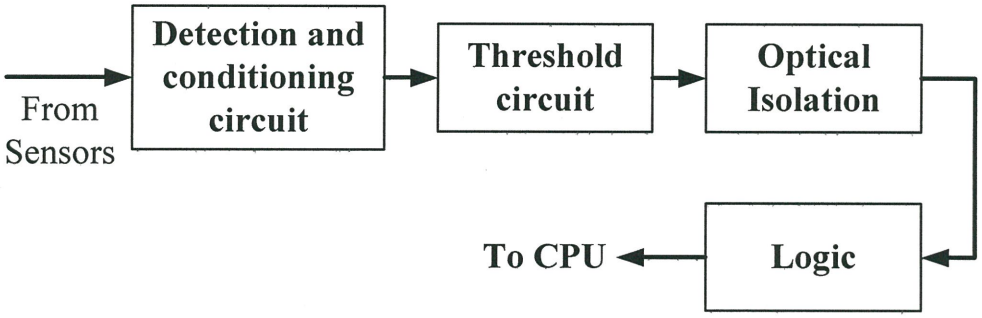

FIGURE Q5(c)

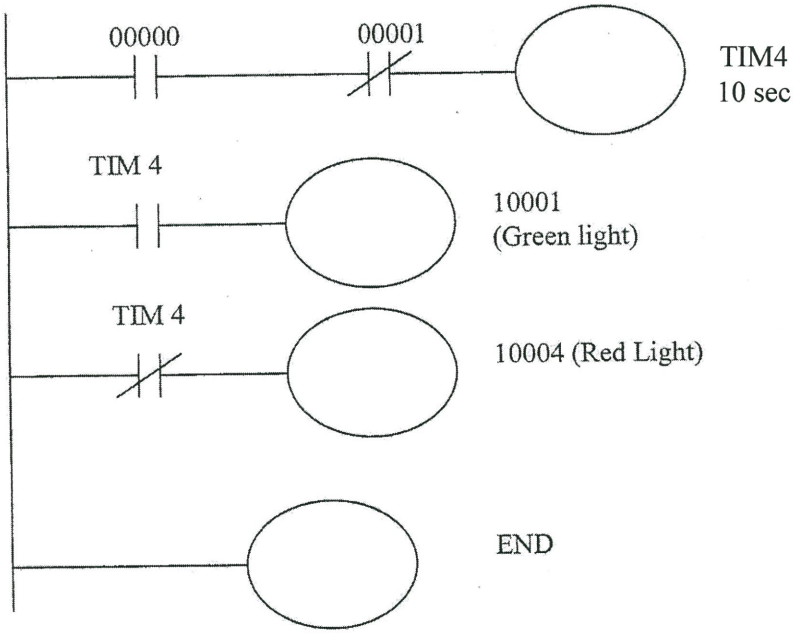

FIGURE Q5(d)

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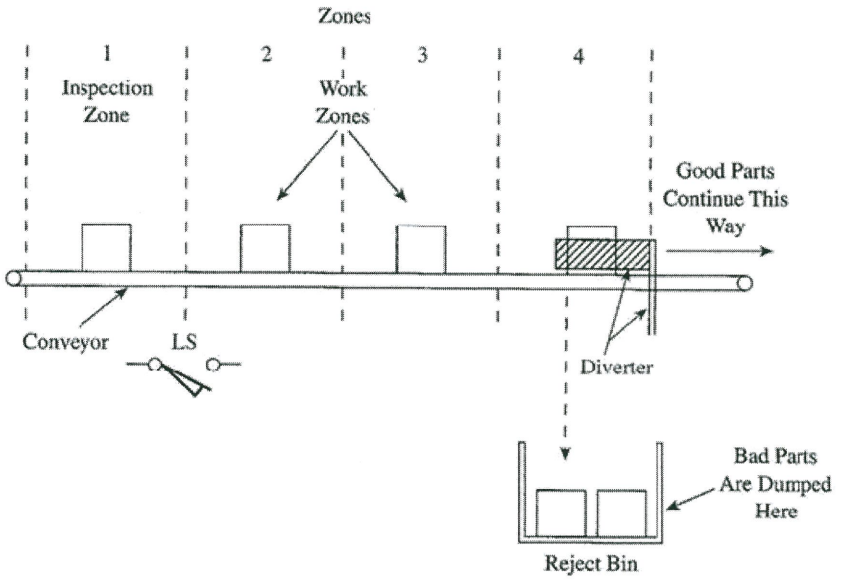
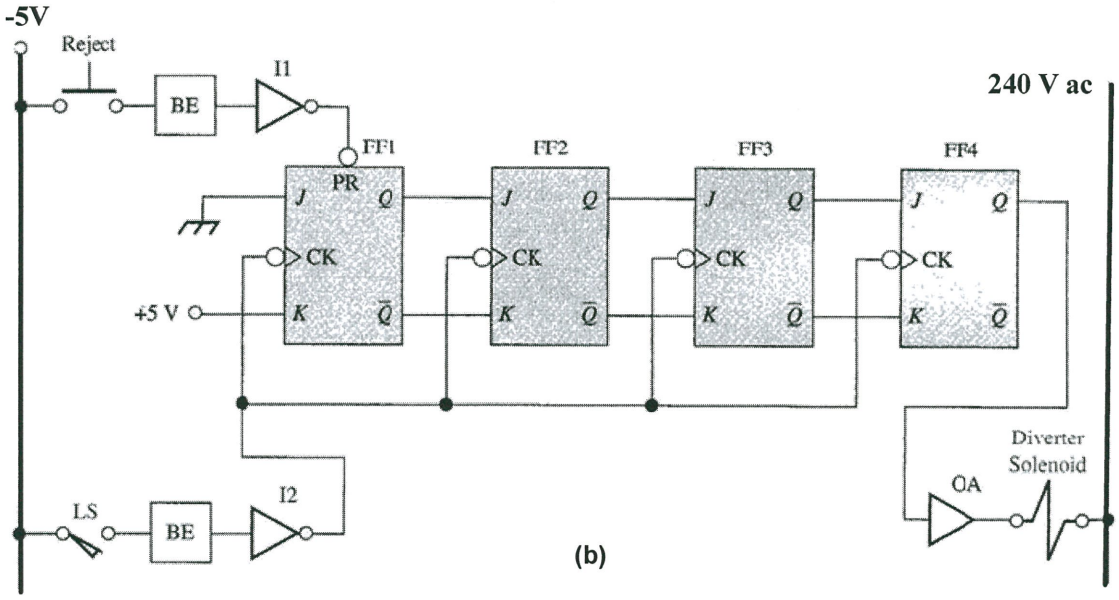


(a)



(b)

FIGURE Q6