Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2014/2015

COURSE NAME	:	DIGITAL DEVICES AND CIRCUITS
COURSE CODE	:	BNR 23103
PROGRAMME	:	2 BNE
EXAMINATION DATE	:	JUNE / JULY 2015
DURATION	:	3 HOURS
INSTRUCTION	:	1. ANSWER **ALL** QUESTIONS FROM **SECTION A** AND ANY **TWO (2)** QUESTIONS FROM **SECTION B**. 2. ATTACH **APPENDIX A** AND **B** WITH YOUR ANSWER BOOKLET

THIS QUESTION PAPER CONSISTS OF **TWELVE (12)** PAGES

SECTION A

Q1 (a) Describe the main advantage of parallel transfer over serial transfer of binary data.
(2 marks)

(b) Perform the following operation:
(i) $10001100_2 + 00111001_2$
(ii) $C8_{16} - 3B_{16}$
(iii) BCD number: 10011000 + 10010111
(6 marks)

(c) Using Boolean Algebra, prove that:
$$\overline{A}\,\overline{B}C + (\overline{A + B + \overline{C}}) + \overline{A}\,\overline{B}\,\overline{C}D = \overline{A}\,\overline{B}C + \overline{A}\,\overline{B}D$$

Given rules of Boolean Algebra:
$(A+0=A,\ A+1=1,\ A+A=A,\ A+\overline{A}=1,\ A+\overline{A}B=A+B)$
(4 marks)

(d) **Figure Q1(d)** shows a combinational logic circuit. From the figure:
(i) write the Boolean expression for output X and simplify it using De Morgan Theorem.
(4 marks)

(ii) determine the value of output X for all possible input conditions and list the values in a truth table.
(4 marks)

Q2 (a) Explain the difference between sum-of-product (SOP) and product-of-sum (POS) expressions.
(2 marks)

(b) Use Karnaugh map to simplify the following expression to minimum POS form:
$$F = (X + Y)(W + Z)(X + Y + \overline{Z})(W + X + Y + Z)$$
(4 marks)

(c) **Figure Q2(c)** shows the inputs and output patterns of a logic circuit. The inputs are WXY and the output is Z.
(i) Obtain the truth table for this circuit.
(4 marks)

(ii) Write the output expression in SOP form.
(3 marks)

(iii) Simplify the output expression using Karnaugh map and implement this circuit using NAND gates ONLY.
(7 marks)

Q3 (a) (i) Briefly explain what is meant by a decoder.
(ii) State the difference between a decoder and an encoder.
(4 marks)

(b) **Table Q3(b)** shows the truth table of a combinational logic circuit.
(i) Draw the gate using ONLY a 4:1 multiplexer and an inverter.
(6 marks)

(ii) Draw the gate using ONLY one 74x151 8:1 multiplexer chip with input/output as shown in **Figure Q3(b)**.
(6 marks)

(c) Use the 74138 IC as depicted in **Figure Q3(c)** to implement the following function.

$$W = A\overline{B}\,\overline{C} + C + AB$$

$$Y = AC + AB + \overline{A}B\overline{C} + \overline{A}\,\overline{C}$$

(4 marks)

SECTION B

Q4 (a) What are the differences between latch and flip-flop? List three types of latches and flip-flop.
(4 marks)

(b) With the aid of truth tables, describe the differences among the following flip-flops.
(i) RS flip-flop
(ii) JK flip-flop
(iii) D flip-flop
(6 marks)

(c) Sketch the gate-level circuit for a NOR-based SR latch.
(4 marks)

(d) **Figure Q4(d)(i)** shows a logic circuit that comprises of a D latch and a D flip-flop, while **Figure Q4(d)(ii)** shows the waveform for signal *CLK* and *D*. Complete the timing diagram for Q_a and Q_b in **APPENDIX A**.
(6 marks)

Q5 (a) Describe the difference between an **asynchronous** and a **synchronous** counter with the aid of diagram/figures.

(3 marks)

(b) (i) Explain the difference between a counter and a shift register.

(ii) State two principal functions performed by a shift register.

(3 marks)

(c) Design a counter to produce the following sequence of 00, 10, 01, 11, 00...using J-K flip-flops. Your design should include next-state table, transition table, Karnaugh-map simplification and implementation of logic circuit.

(7 marks)

(d) Develope the diagram of all the Q_s (Q_0 to Q_3) output waveforms for a 74HC195 4-bit shift register when the inputs are as shown in **Figure Q5(d)**.

(7 marks)

Q6 (a) Two 4-bit numbers ($A_3A_2A_1A_0$ = 1101 and $B_3B_2B_1B_0$ = 1011) are applied for a 74LS83A 4-bit parallel adder. **Figure Q6(a)** shows the 74LS83A IC. The input carry is 1. Determine the sum, Σ and the output carry, C_4.

(4 marks)

(b) For each set of binary numbers, determine the output states for the comparator of **Figure Q6(b)**:

(i) $A_3A_2A_1A_0 = 1100$ and $B_3B_2B_1B_0 = 1001$

(ii) $A_3A_2A_1A_0 = 1000$ and $B_3B_2B_1B_0 = 1011$

(iii) $A_3A_2A_1A_0 = 0100$ and $B_3B_2B_1B_0 = 0100$

(6 marks)

(c) Design the block diagram for the Mealy and Moore state machine.

(3 marks)

(d) **Figure Q6(d)** shows the state diagram for a 3-bit up/down code counter. From the state diagram, derived the next state table for the 3-bit up/down code counter.

(7 marks)

- END OF QUESTION –

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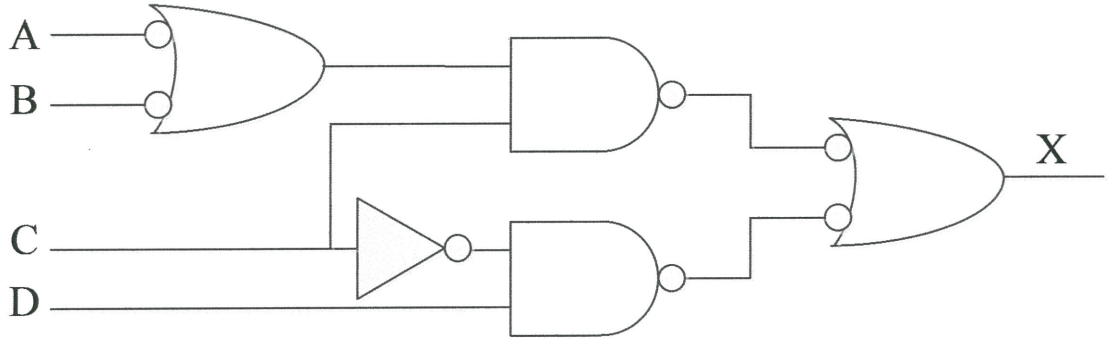

FIGURE Q1(d)

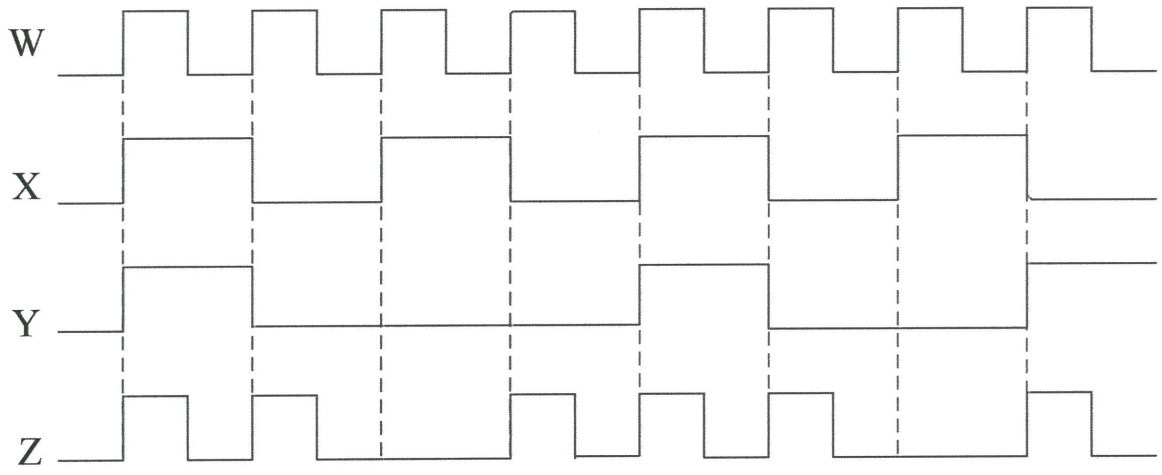

FIGURE Q2(c)

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A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

TABLE Q3(b)

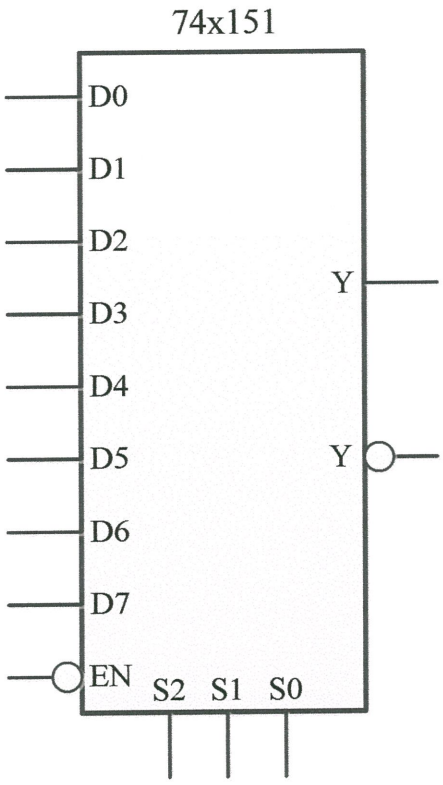

FIGURE Q3(b)

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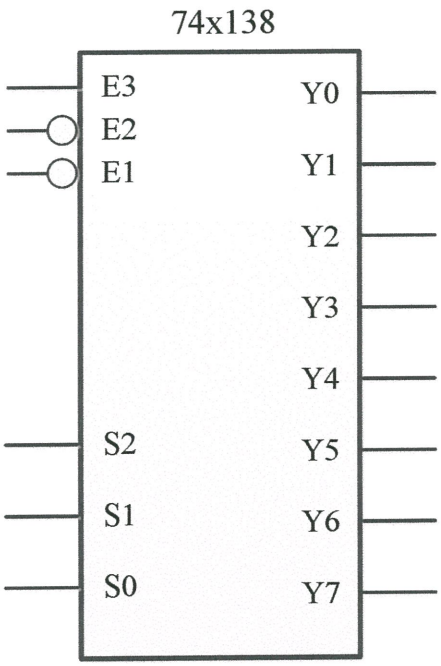

FIGURE Q3(c)

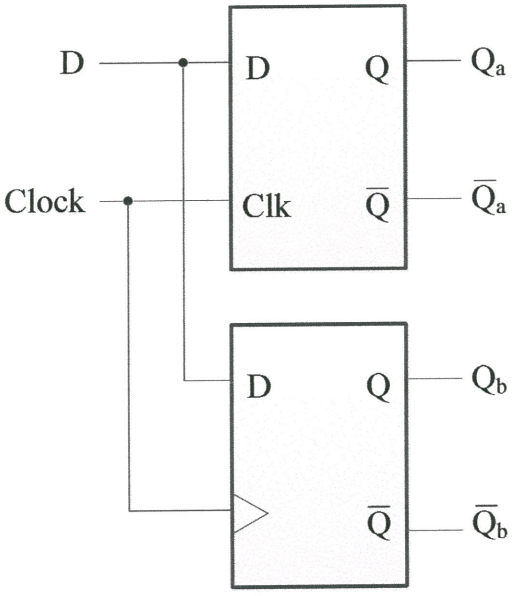

FIGURE Q4 (d)(i)

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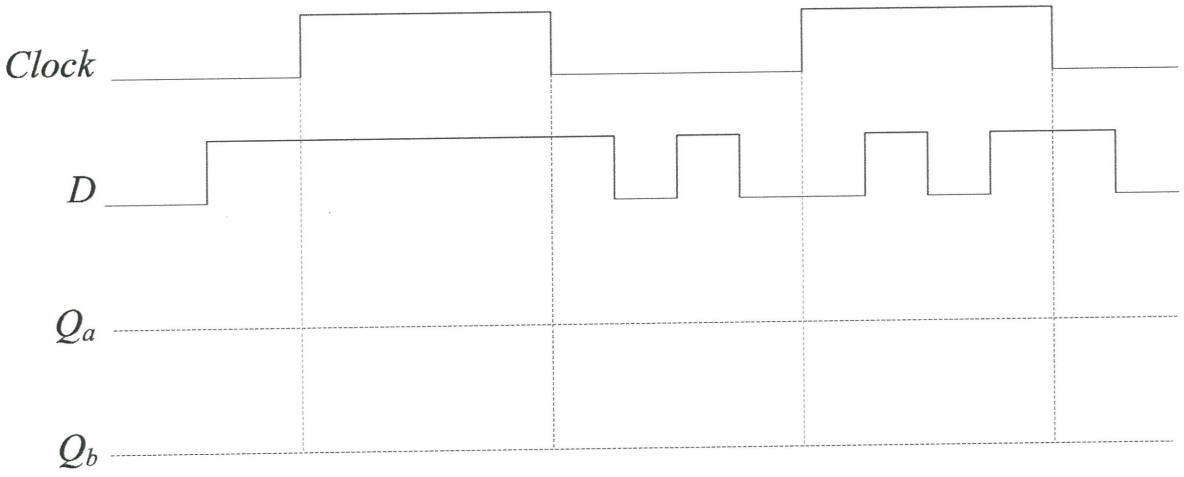

FIGURE Q4 (d)(ii)

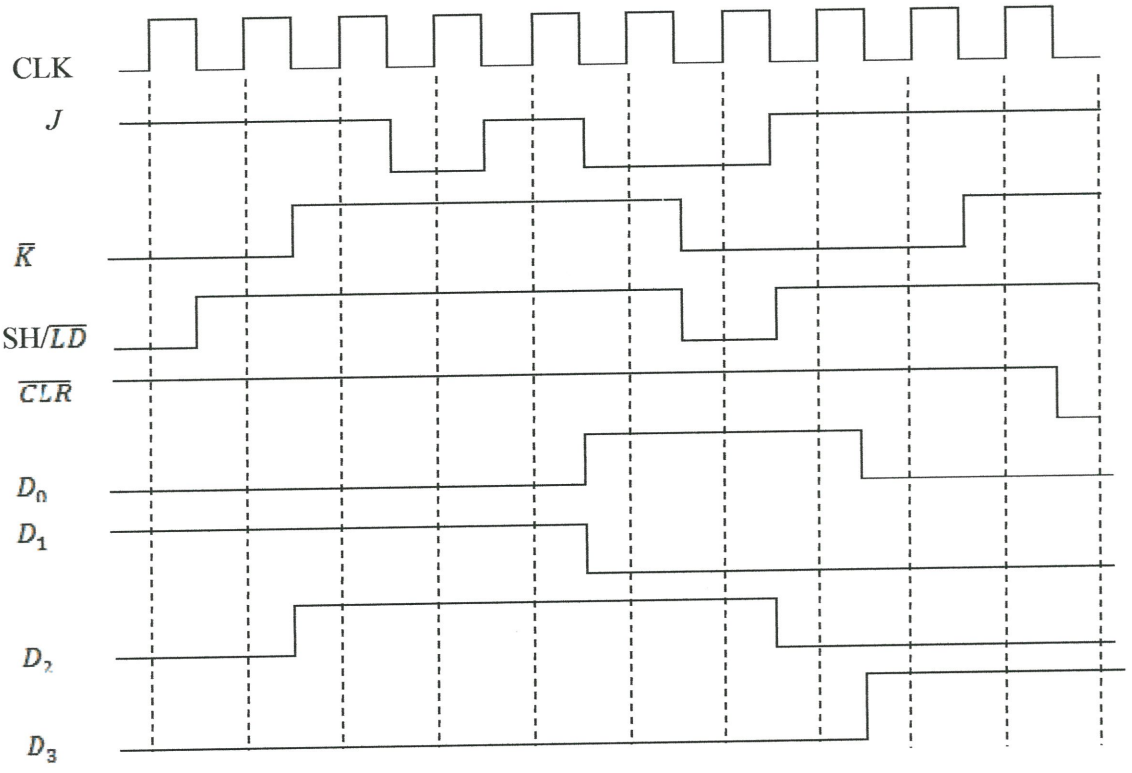

FIGURE Q5(d)

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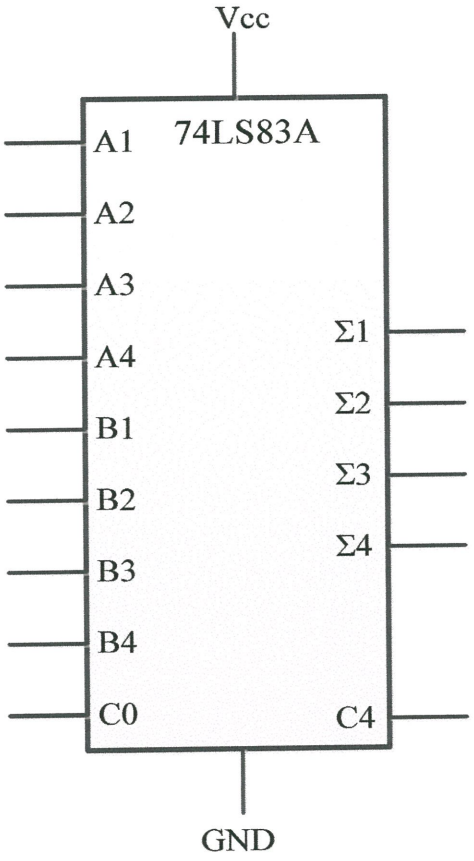

FIGURE Q6 (a)

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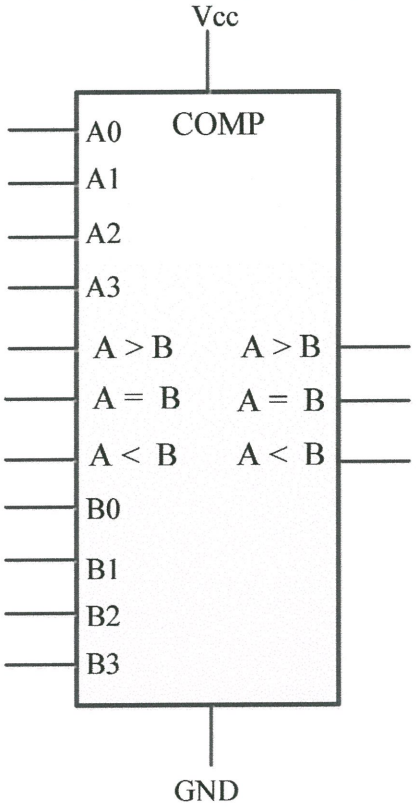

FIGURE Q6 (b)

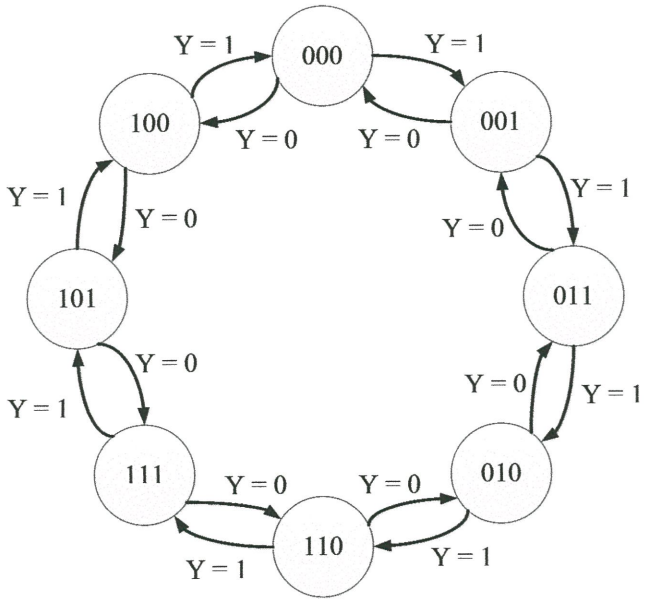

FIGURE Q6 (d)

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APPENDIX A

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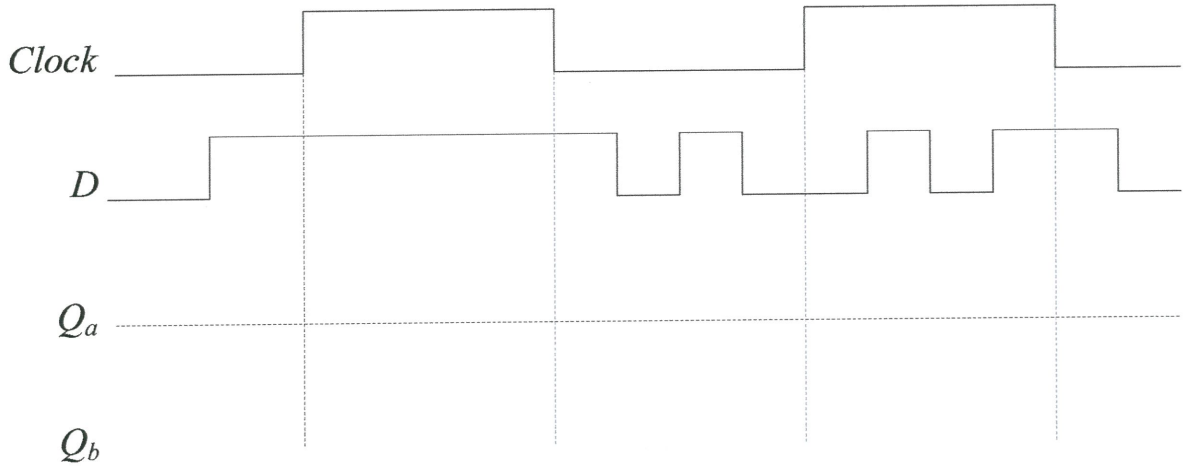
MATRIC NO. : _____



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APPENDIX B

NAME : _____

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