Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2019/2020

COURSE NAME	:	COMPUTER ARCHITECTURE AND ORGANIZATION
COURSE CODE	:	BEC30303
PROGRAMME CODE	:	BEJ
EXAMINATION DATE	:	DECEMBER 2019/JANUARY 2020
DURATION	:	3 HOURS
INSTRUCTION	:	ANSWER ALL QUESTIONS IN **SECTION A** **IN OMR SHEET** AND ALL QUESTIONS IN **SECTION B** **IN THE QUESTION BOOKLET**

THIS QUESTION PAPER CONSISTS OF **THIRTEEN (13)** PAGES

SECTION A: OBJECTIVE QUESTIONS (15 MARKS)

Q1 Three (3) factors affect the performance of a computer are:
a) Hardware design, Instruction set, Compiler
b) Hardware design, Speed, Cost
c) Speed, Cost, Memory management
d) Speed, Cost, Compiler

Q2 Integrated circuit is on _____ generation in computer evolutions.
a) First
b) Second
c) Third
d) Fourth

Q3 A data bus is _____.
a) Bidirectional
b) Providing a path for communication between the processor and other devices
c) To transfer bits of a word in parallel
d) All of the mentioned

Q4 _____ converts the programs written in assembly language into machine instructions.
a) Machine compiler
b) Interpreter
c) Assembler
d) Converter

Q5 What is not true about RISC?
a) A large number of addressing mode
b) Simple instruction
c) Hardware control unit
d) A single chip processor

Q6 The prefix expression for (A + B) * C + D / (E + F * G) – H is
a) + + A B * C / D + E * F G - H
b) - + * + A B C / D + E * F G H
c) - * + A B C / + D + E * F G H
d) * + A B C / + D + E * F G - H

Q7 Construct the infix for / - A B * C ^ D E
a) A – B / C ^ D * E
b) A – B * C / D ^ E
c) (A – B) / (C * D ^ E)
d) A – (B * C ^ D) / E

Q8 The postfix for / + - A / B C E + A B
a) A B C / + E – A B + /
b) A B / C E – A B + + /
c) A B / C E - + A B + /
d) A B C / - E + A B + /

Q9 Which addressing mode is used for initialization of the variable?
a) Indexed addressing
b) Direct addressing
c) Register addressing
d) Immediate addressing

Q10 Determine the addressing modes for DIV R5, #3
a) Indexed addressing
b) Direct addressing
c) Register addressing
d) Immediate addressing

Q11 The meaning of ADD R2, (2002) is
a) R2 <- R2 + 2002
b) R2 <- R2 + M[2002]
c) R2 <- M[R2] + M[2002]
d) R2 <- M[R2] + 2002

Q12 Device synchronization can be done by_____.
a) program controlled I/O
b) interrupt driven
c) direct memory access
d) All the above

Q13 The time between the receiver of an interrupt and its service is _____.
a) Trace mode delay
b) Interrupt latency
c) Cycle time
d) Switching time

Q14 Interrupts form an important part in _____ systems.
a) real-time processing
b) memory
c) CPU
d) bus

Q15 General purpose register can be used for _____.
a) Holding data
b) Holding address
c) Both A and B
d) None

Q16 Cache memory acts between_____.
a) CPU and RAM
b) RAM and ROM
c) CPU and Hard Disk
d) Primary Storage and Secondary Storage

Q17 The ROM chips are mainly used to store _____.
a) System files
b) Root directories
c) Boot files
d) Driver files

Q18 The effectiveness of the cache memory is based on the property of _____.
a) Memory size
b) Locality of reference
c) Memory localization
d) None of the mentioned

Q19 If a magnetic disc has 100 cylinders, each containing 10 tracks of 10 sectors, and each sector can contain 128 bytes, what is the maximum capacity of the disk in bytes?
a) 128
b) 1280
c) 12800
d) 1280000

Q20 The disadvantage of the primary storage is
a) The high cost factor
b) The low efficiency
c) The low speed of operation
d) The need to remove the chip physically to reprogram it

Q21 The PROM is more effective than ROM chips in regard to _____ .
a) Cost
b) Memory management
c) Speed of operation
d) Both Cost and Speed of operation

Q22 The memory devices which are similar to EEPROM but differ in the cost effectiveness is _____ .
a) Memory sticks
b) Blue-ray devices
c) CMOS
d) Flash memory

Q23 The standard SRAM chips are costly as _____ .
a) They use highly advanced micro-electronic devices
b) They house 6 transistor per chip
c) They require specially designed PCB's
d) None of the mentioned

Q24 The average number of steps taken to execute the set of instructions can be made to be less than one by _____ .
a) ISA
b) Super Scaling
c) Non-pipeline
d) CISC

Q25 In pipelining the task which requires the least time is performed first.
a) True
b) False

Q26 To increase the speed of memory access in pipelining, we make use of _____ .
a) Special memory locations
b) Special purpose registers
c) Cache
d) Buffer

Q27 The extra time needed to bring the data into memory in case of a miss is called as _____.
a) Delay
b) Propagation time
c) Miss penalty
d) None of the mentioned

Q28 The suitable wireless connection for short ranged connectivity is:
a) Bluetooth
b) WiFi
c) ZigBee
d) 3G

Q29 IoT evolved _____ connection.
a) machine to machine
b) man to man
c) man to machine
d) machine to man

Q30 All the statement below are the advantage of IoT except _____.
a) vulnerability of the data
b) generate more revenue
c) improve user experience
d) integrating business model

SECTION B: SUBJECTIVE QUESTIONS (85 MARKS)

Q31 (a) Assume that there are three microprocessors using CISC instruction set with different instruction format. Each microprocessor requires different amount of time to execute the instruction as shown on **Table Q31(a)**. Which microprocessor is the fastest to perform the operation:

$$A = B + C * (\frac{D}{E})$$

Table Q31(a)

Microprocessor	Instruction Type	Time per instruction
CPU 3	Three-address instructions	80 ns
CPU 2	Two-address instructions	50 ns
CPU 1	One-address instructions	40 ns

Instruction Type	Instruction Code	Total Time
Three-address instructions – CPU3		
Two-address instructions – CPU2		
One-address instructions - CPU1		
The fastest CPU performances is:		

(10 marks)

(b) Determine the type of addressing modes for the following instructions:

Instruction	Addressing Modes
LOAD R1, (R2+R3+200)	
LOAD R1, (0 X 1122AABB)	
MOV A, 18H	
MOV BX, CX	

(2 marks)

Q32 (a) Explain two reasons on why an interrupt is occurred.

(2 marks)

(b) Describe the drawbacks of an interrupt?

(2 marks)

(c) Differentiate between Interrupt and Exceptions in terms of handling the error.

(3 marks)

(d) Explain how a debugger analyse the Exceptions occurred in a system.

(3 marks)

Q33 Write the sequence of actions required for the bus in **Figure Q33** for the following instructions;

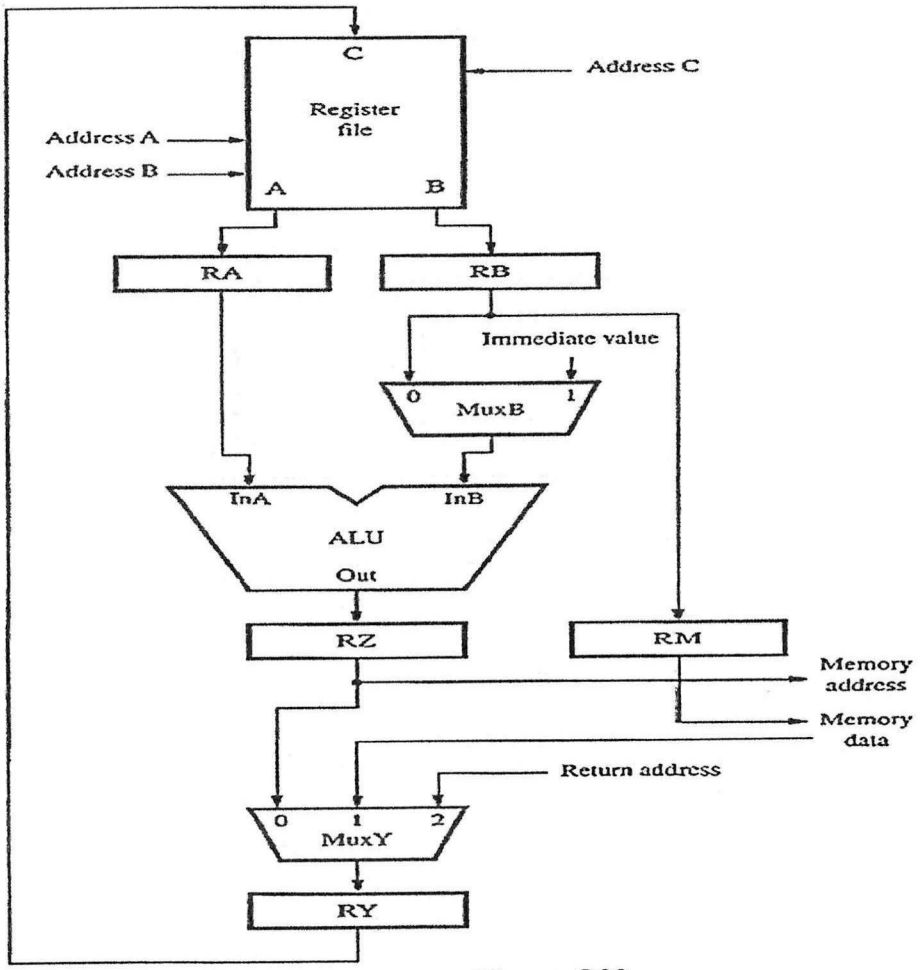

Figure Q33

(a) MUL R22, R33

(5 marks)

(b) Load R5, X(R7)

(5 marks)

Q34 (a) Compare two (2) major differences between Primary Storage and Secondary Storage.

(2 marks)

(b) Differentiate between PROM and EPROM in terms of its characteristic.

(1 mark)

Q35 Consider a machine with addressable 16-bit memory with 1 byte on each block. Illustrate the flow of instruction execution process that may happens in memory, control unit and Arithmetic Logic Unit (ALU) when processing the following instruction:

```
LOAD R1, (20);
LOAD R2, (30);
ADD R1,R2;
STORE X, R1;
```

(5 marks)

Q36 (a) By using the features as in **Table Q36(a),** determine the miss penalty in nanoseconds when a L2 cache miss occurs. Assume that the duration for 1 clock cycle is 5 ns.

Table Q36(a)

Memory Type	Clock Cycle
L1 cache	2
L2 cache	6
L3 cache	8
DDR SDRAM	143
Hard disk	178

(3 marks)

(b) By using the features as in **Table Q36(a)** and **Table Q36 (b)**, calculate the;

Table Q36(b)

Item	Value
Total Number of L2 Cache accessed by CPU	20 access
Total Number of Hit	18 access
Hit Time	6 ns

(i) Hit rate of the system

(2 marks)

(ii) Miss Rate of the system

(2 marks)

(iii) Average Memory Access Time of the system

(3 marks)

(c) If the L2 cache is replaced with new cache with performance of 97% hit rate and 5 ns hit time, calculate the new Average Memory Access Time for this system.

(4 marks)

Q37 Assume that a pipeline system use 1 cycle to perform Fetch (F), 1 cycle to perform Decode (D), 2 cycle to perform Execution (E), 1 cycle to perform Write Back (W). Assume that 1 clock cycle takes 5 ns. Assume that a program segment needed to be processed is as below:

```
MOV R1, #500;
MOV R2, #25;
DIV R1, R2;
STORE R3, R1;
```

(2 marks)

(b) Sketch the space time diagram to execute these four (4) instructions.

(5 marks)

(c) Calculate the total execution time needed by the pipelined computer to execute a JAVA code that having 3505 instructions.

(4 marks)

(d) Calculate the performance speed up of the pipelined computer over non-pipelined computer to execute similar C++ program in **Q37(c).**

(4 marks)

Q38 The following measurements are recorded on a machine that running a given set of benchmark program with clock rate of 200MHz.

Instruction Types	Instruction Count	Cycle per Instruction
Arithmetic and logic	10×10^6	1
Load and store	8×10^6	2
Branch	2×10^6	4
Others	4×10^6	3

Calculate:

(a) Total cycle to complete all the instructions

(2 marks)

(b) Total instruction (I_c)

(2 marks)

(c) Cycle per Instruction (CPI)

(2 marks)

(d) Million Instruction per Cycle (MIPS)

(2 marks)

(e) Instruction time (CPU)

(2 marks)

Q39 (a) Explain why the IoT system is always referred as 'Machine-to-Machine' communication and being predicted will take over several human jobs.

(2 marks)

(b) Discuss the advantages and disadvantages of IoT system.

(4 marks)

- END OF QUESTIONS –