Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2019/2020

COURSE NAME	: VLSI DESIGN
COURSE CODE	: BED 30303
PROGRAMME CODE	: BEJ
EXAMINATION DATE	: DECEMBER 2019/JANUARY 2020
DURATION	: 3 HOURS
INSTRUCTION	: 1. ANSWER **ALL** QUESTIONS 2. ATTACH APPENDIX SHEET WITH ANSWER BOOKLET

THIS QUESTION PAPER CONSISTS OF **SIX (6)** PAGES.

Q1 (a) Integrated circuits also known as ICs, chips or microchips. IC technology is able to integrate a complex set of electronic components and their interconnections on a small semiconducting material.

(i) Justify **FOUR (4)** reasons why IC technology is commonly used to create modern electronic systems.

(4 marks)

(ii) Discuss **THREE (3)** applications of integrated circuits.

(6 marks)

(b) Complementary Metal Oxice Semiconductor (CMOS) is one of logic families that could be used to design logic circuit.

(i) Sketch general structure of CMOS circuit and its truth table.

(4 marks)

(ii) CMOS circuit is suitable for developing battery-powered devices. Justify why.

(4 marks)

(iii) Discuss **TWO (2)** limitations of CMOS logic circuit.

(2 marks)

Q2 (a) **Figure Q2(a)** illustrates top view of a CMOS circuit. Analyze the top view CMOS circuit and sketch the cross sectional view for the figure.

(10 marks)

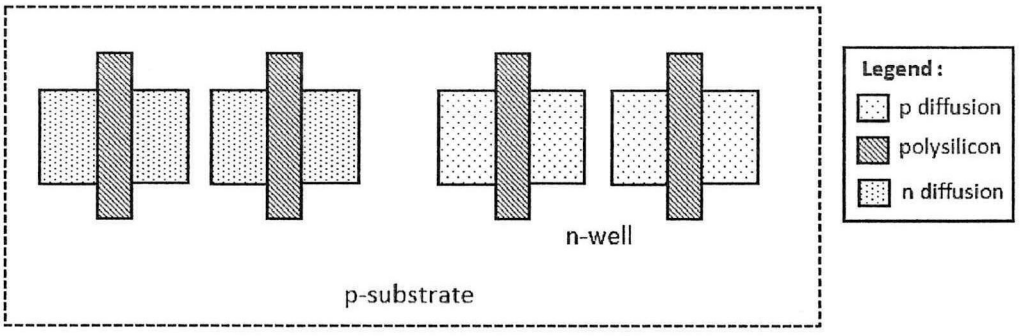

Figure Q2(a)

(b) Briefly explain stick diagram and its role in VLSI circuit.

(4 marks)

(c) Discuss all basic rules for drawing a stick diagram.

(6 marks)

Q3 **Figure Q3** shows a CMOS logic circuit.

(a) Define euler path.

(2 marks)

(b) Sketch the euler path.

(8 marks)

(c) Construct the stick diagram.

(10 marks)

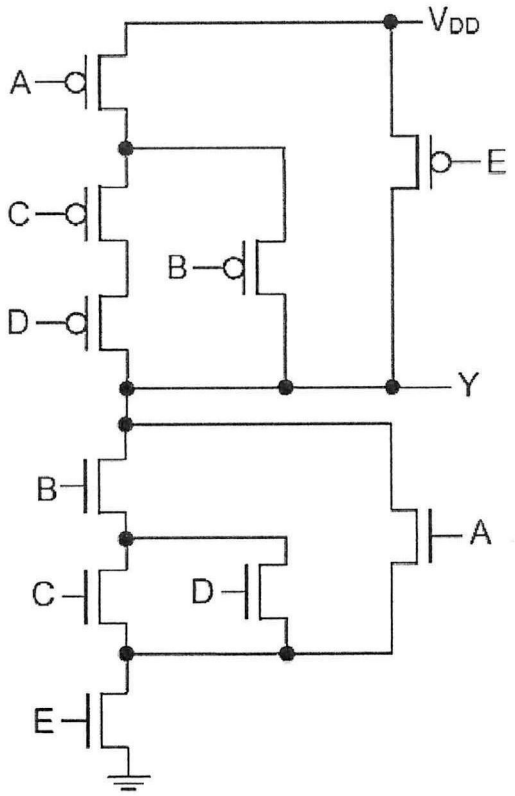

Figure Q3

Q4 (a) With the aide of diagram, briefly explain the operation characteristic of a MOSFET in **THREE (3)** regions.

(9 marks)

(b) Determine operating region of the transistors for a CMOS inverter when the input of the CMOS inverter is equal to inverter threshold voltage, V_{th}.

(2 marks)

(c) Examine major sources of power dissipation in a CMOS logic circuit. Justify your answer.

(5 marks)

(d) The short circuit power is due to the finite rise time and fall time of the input signal. It contributes significant towards dynamic power. Suggest **TWO (2)** methods to reduce short circuit current.

(4 marks)

Q5 (a) A circuit for a gated D latch is shown in **Figure Q5(a)(i)**.

(i) Draw transistor circuit for the logic circuit in **Figure Q5(a)(i)** using static CMOS.

(8 marks)

(ii) Complete the timing diagram **Figure Q5(a)(ii)** given in **APPENDIX I**. Attach the appendix sheet with answer booklet.

(4 marks)

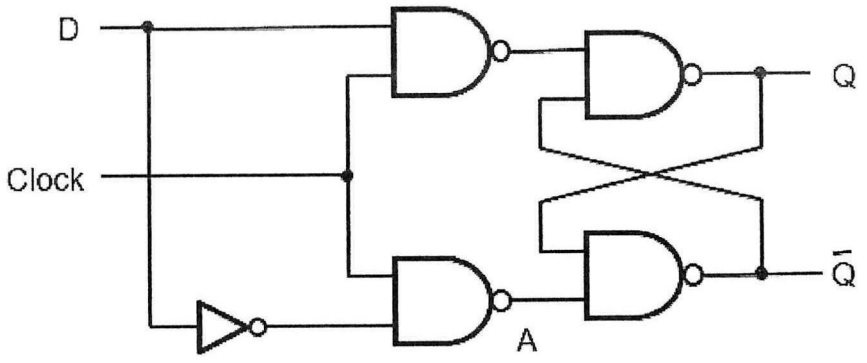

Figure Q5(a)(i)

(b) **Figure Q5(b)** shows the implementation of the function $S = A\bar{B} + \bar{A}B$ using pass transistor logic.

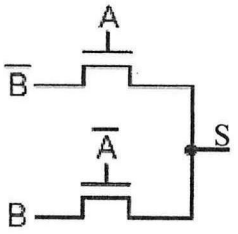

Figure Q5(b)

(i) Analyze and describe the limitation of transistor circuit in **Figure Q5(b)**.

(4 marks)

(ii) Propose a solution to overcome the limitation as mentioned in **Q5(b)(i)**. Redraw the logic circuit in **Figure Q5(b)** with the proposed solution.

(4 marks)

- END OF QUESTIONS –

APPENDIX I

FINAL EXAMINATION

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Figure Q5(a)(ii)