

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION **SEMESTER I SESSION 2019/2020**

COURSE NAME

: MICROFABRICATION

COURSE CODE

: BED 40603

PROGRAMME CODE : BEJ

EXAMINATION DATE : DECEMBER 2019/ JANUARY 2020

DURATION

: 3 HOURS

INSTRUCTION

: ANSWER ALL QUESTIONS

THIS QUESTION PAPER CONSISTS OF FOUR (4) PAGES

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Q1 (a) (i) List the basic processes involved in fabricating ICs using planar technology.

(6 marks)

(ii) List the steps used in the preparation of Silicon to wafers.

(5 marks)

(b) (i) Explain the term epitaxy growth in IC fabrication.

(2 marks)

(ii) Describe the basic chemical reaction in the epitaxial growth process of pure silicon.

(6 marks)

(iii) Sketch a simple chemical vapour deposition reactor that used for epitaxy layer.

(6 marks)

Q2 (a) (i) Describe thermal oxidation process.

(3 marks)

(ii) State TWO (2) important properties of SiO₂.

(2marks)

(iii) Analyse field-oxide formation and gate oxide formation, in term of oxidation process.

(5 marks)

(i) A Si wafer has an unknown initial oxide thickness, x_i. The wafer then goes through a particular oxidation process with a linear oxidation constant B/A = 1.2 μm/hour and a parabolic oxidation constant B = 0.3 μm²/hour. After thermal oxidation for 1 hour, the total oxide thickness is measured to be x μm. With an additional 3 hours of oxidation, the total oxide thickness becomes 2x μm. Find the numerical values of x and x_i.

[Hint: The solution for the quadratic equation $ax^2 + bx + c = 0$].

(15 marks)



- Q3 (a) (i) Briefly explain photolithography process and type of photoresist. (4 marks)
 - (ii) Discuss **TWO** (2) basic components in photoresist. (4 marks)
 - (iii) Explain TWO (2) elements that can contribute to the photoresist thickness during the coating process as shown in Figure Q3(a)(iii).

 (4 marks)

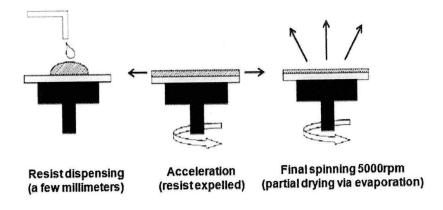


Figure Q3(a)(iii)

(b) As a postgraduate student, design a sputtering system for metallization process. Sketch the design apparatus and explain briefly the sputtering mechanism.

(7 marks)

(c) As a researcher, you have to decide the lab equipment to investigate the topological properties of your thin film. Analyse the equipment needed and their properties.

(6 marks)

- Q4 (a) Diffusion is a process where an exact amount of impurities/dopant atoms is introduced into the semiconductor (Si) material under specific process conditions.
 - (i) Explain **TWO** (2) atomic diffusion mechanism in a twodimensional lattice and explain clearly using approriate diagram. (10 marks)



(b) Copper is proposed as an interconnect material in newer generation of ICs because of its low electrical resistivity. There is no reliable process recipe to etch copper by RIE. Propose and a process flow to fabricate copper interconnects in a planarized multilevel metallization scheme for **Figure Q4** (b).

Starting with a SiO2 layer on Si substrate, show all the step with process description and cross-sections.

(15 marks)

CVD Oxide		
Cu	Cu	CVD Oxide
SiO2		
Substrate		

Figure Q4(b)

- END OF QUESTIONS -