UTHM
Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2019/2020

COURSE NAME	:	DIGITAL ELECTRONICS
COURSE CODE	:	BEL 20303
PROGRAMME CODE	:	BEV/ BEJ
EXAMINATION DATE	:	DECEMBER 2019 / JANUARY 2020
DURATION	:	3 HOURS
INSTRUCTION	:	1. ANSWER **ALL** QUESTIONS IN THIS BOOKLET. 2. **NO CALCULATOR** IS ALLOWED.

THIS QUESTION PAPER CONSISTS OF **FOURTEEN (14)** PAGES

Q1 (a) Describe **THREE (3)** technique to convert decimal number to binary conversion.
(3 marks)

(b) Convert a negative decimal number, **-35** in binary number, 1's and 2's complement form using 8-bit binary.

(6 marks)

(c) Consider a 4-bit binary number function, **F(A B C D)** is represented in **4-bit signed number format**.

(i) Write out the truth table for the Boolean function of F where the absolute value of F is **greater than 2**.

(6 marks)

(ii) Analyze the truth table and write out the **minimum sum-of-product (SOP)** of the Boolean function.

(5 marks)

Q2 (a) Design a circuit that counts the number of 1's present in 3 inputs A, B and C. Its output is a two-bit number which are X_1 and X_0, representing that count in binary.

(i) Construct the truth table for this circuit.

(5 marks)

(ii) Find the minimize logic equations for output X_1 and X_0. Use the Karnaugh map and Boolean algebra to simplify the expressions.

(5 marks)

(b) Given the Boolean expression:

$y = (a + b)(b + c)(\bar{a} + \bar{b})(\bar{b} + \bar{c})$

(i) Construct a truth table for the output, y.

(4 marks)

(ii) Derive the **minimal product-of-sum (MPOS)** for the output, y.
(4 marks)

(iii) Implement the simplest Boolean expression for the output, y.
(2 marks)

Q3 (a) Describe the operation of the following functional combinational logic circuit. Use an appropriate diagram and a truth table to aid your explanation.

(i) Comparator.

(4 marks)

(ii) Demultiplexer.

(4 marks)

(b) System A, which has three inputs (A3, A2, A1) is designed to produce two outputs, M and N. The output M is **HIGH** whenever A1 and A2 are **HIGH**. Output N is **HIGH** when M and A3 are both **HIGH** or A1 and M are both **LOW**.

A 3 to 8 line decoder shown in **Figure Q3(b)** is used to employ this system together with the external logic gates. Show all the steps to design system A including truth table.

(6 marks)

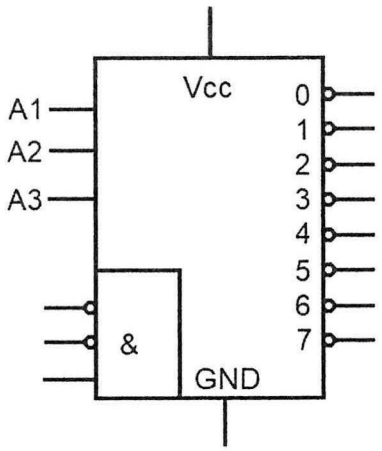


Figure Q3(b)

(c) Evaluate the output for a 4-bit compactor (74LS85) in **Figure Q3(c)** using given inputs of A0, A1, A2, A3, B0, B1, B2 and B3 below. The outputs are active-HIGH.

(6 marks)

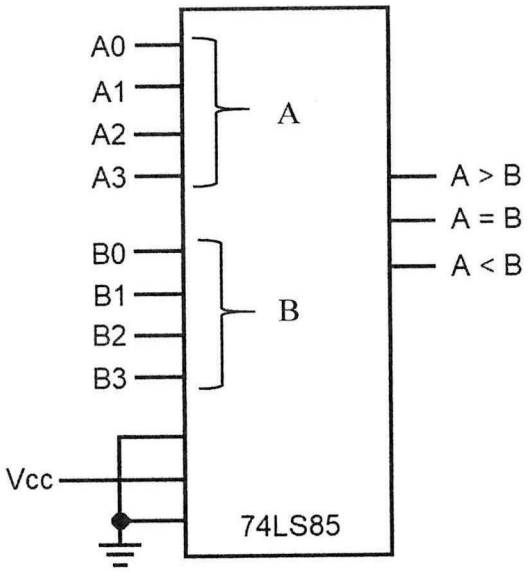
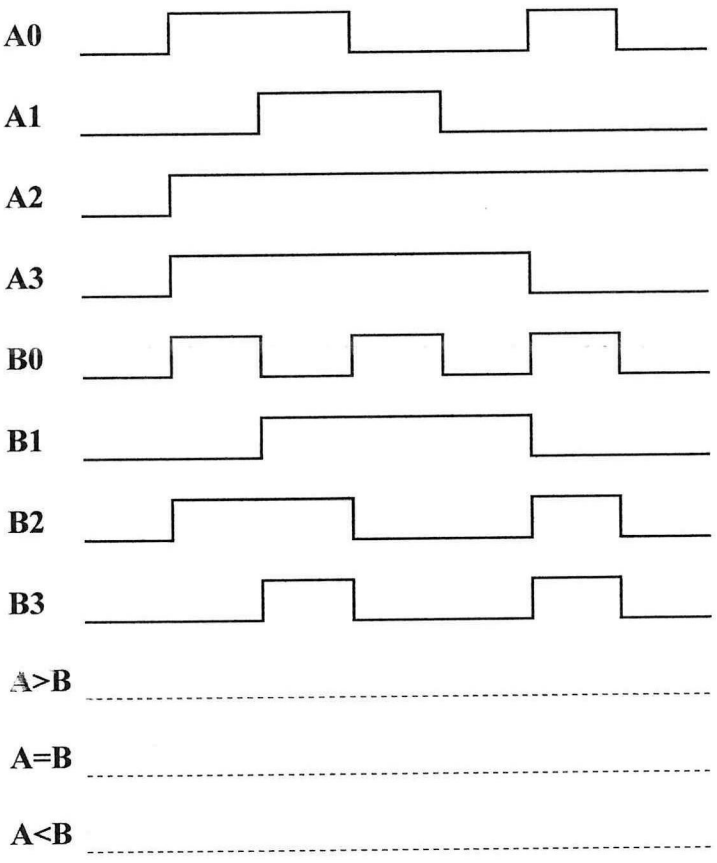


Figure Q3(c)



Q4 (a) Complete the missing entries (i) to (vii) in **Table Q4(a)** of flip-flop excitation values required to produce the indicated flip-flop state changes. X indicates the present state and Y is the desired next state of the flip-flop.

(7 marks)

Table Q4(a)

Present state	**Next State**	**J-K Flip flop**		**SC Flip flop**		**D Flip flop**
X	**Y**	**J**	**K**	**S**	**C**	**D**
0	0	(i)	(ii)			(iii)
(iv)	0	1	1			
0	1			(v)	(vi)	
1	(vii)	1	0			

(b) A clock generator has an output frequency of 112 kHz. The system is required to generate two frequencies, 28 kHz and 7 kHz at the outputs. Design a circuit that will generate the two output frequencies by using JK flip-flops.

(4 marks)

(c) **Figure Q4(c)(i)** shows a register and **Figure Q4(c)(ii)** shows the input waveforms (CLOCK and Data in) to the circuit.

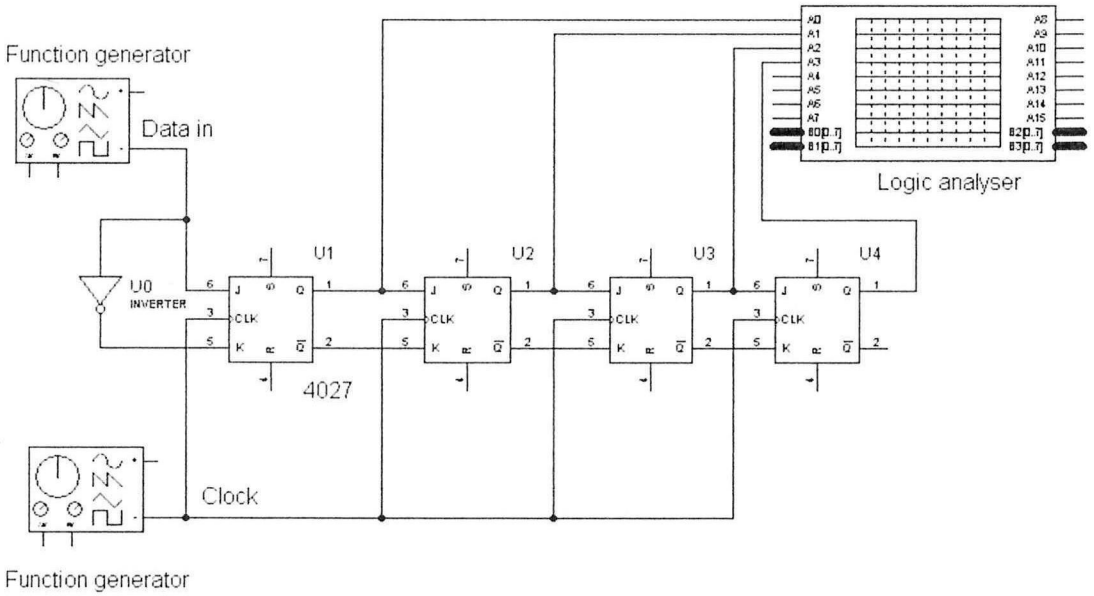


Figure Q4(c)(i)

(i) State the type of register as shown in **Figure Q4(c)(i)**.

(1 marks)

(ii) Analyze the circuit and draw the output waveforms for Q_{U1}, Q_{U2}, Q_{U3} and Q_{U4} in **Figure Q4(c)(ii)**.

(8 marks)

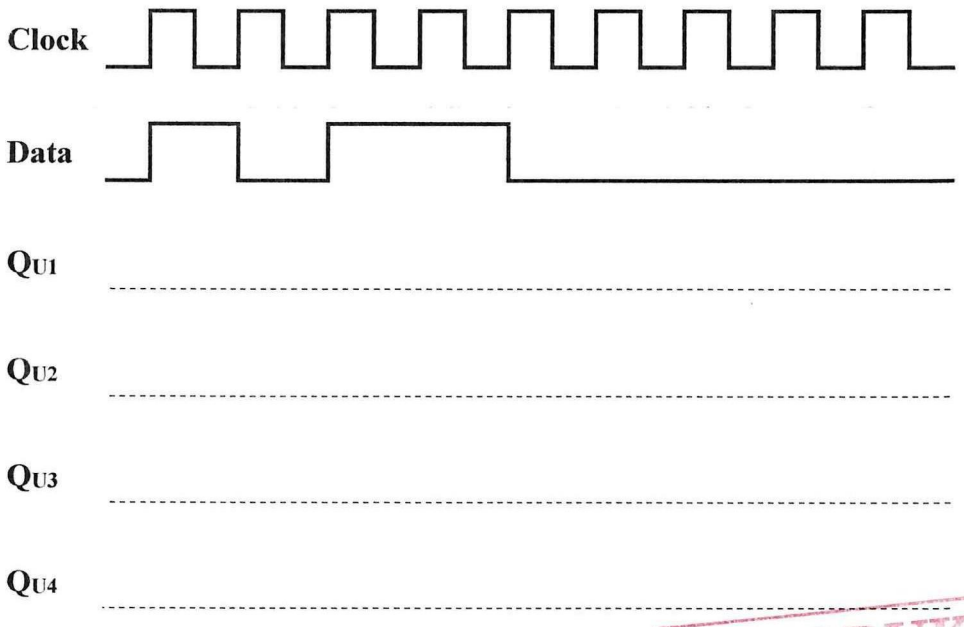


Figure Q4(c)(ii)

Q5 (a) **Figure Q5(a)** shows the state transition diagram of a state machine.

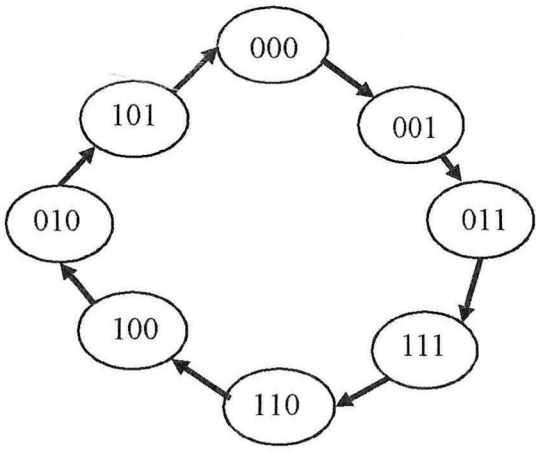


Figure Q5(a)

(i) Build the excitation table for this state machine.

(5 marks)

(ii) Find the simplest Boolean expression for the circuit using Karnaugh map.
(10 marks)

(iii) Implement the circuit diagram based on the result in **Q5(a)(ii)**.

(5 marks)

- END OF QUESTIONS-