Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2018/2019

COURSE NAME	:	VLSI DESIGN
COURSE CODE	:	BED 30303
PROGRAMME	:	BEJ
EXAMINATION DATE	:	DECEMBER 2018/ JANUARY 2019
DURATION	:	3 HOURS
INSTRUCTION	:	ANSWER **ALL** QUESTIONS IN THIS BOOKLET.

THIS QUESTION PAPER CONSISTS OF ELEVEN (11) PAGES

Q1 (a) Justify a modification to transistors dimension that could increase their performance.

(4 marks)

(b) Explain the reason that we usually implement the Pull-Up Network with PMOS and Pull-Down Network with NMOS. (You can show it by drawing the figure of the CMOS inverter.)

(5 marks)

(c) **Figure Q1(c)** shows the transistor level gate configuration for function OUT. Analyse and obtain the Boolean expression for OUT.

(6 marks)

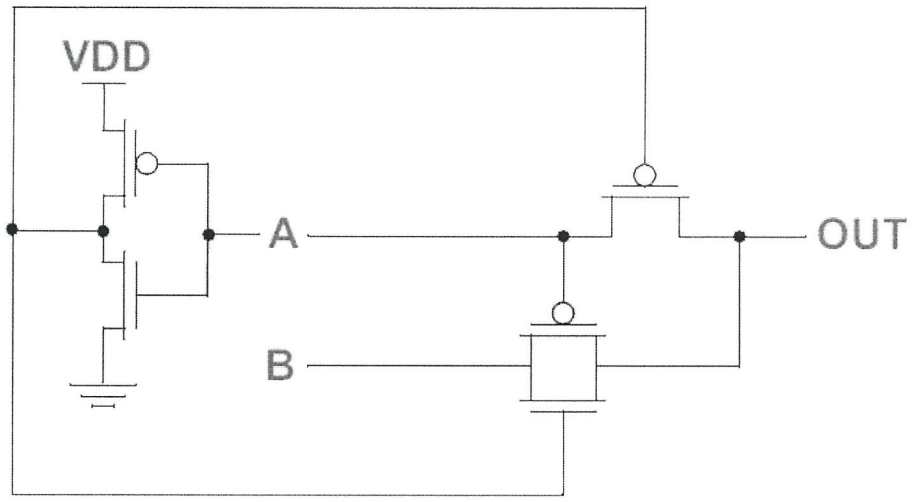

Figure Q1(c)

(d) **Figure Q1(d)** shows a stick diagram of logical circuit using fully complementary static CMOS. Analyse the figure and draw the electrically equivalent transistor level schematic of the stick diagram. Determine the logic equation for the output *OUT*.

(10 marks)

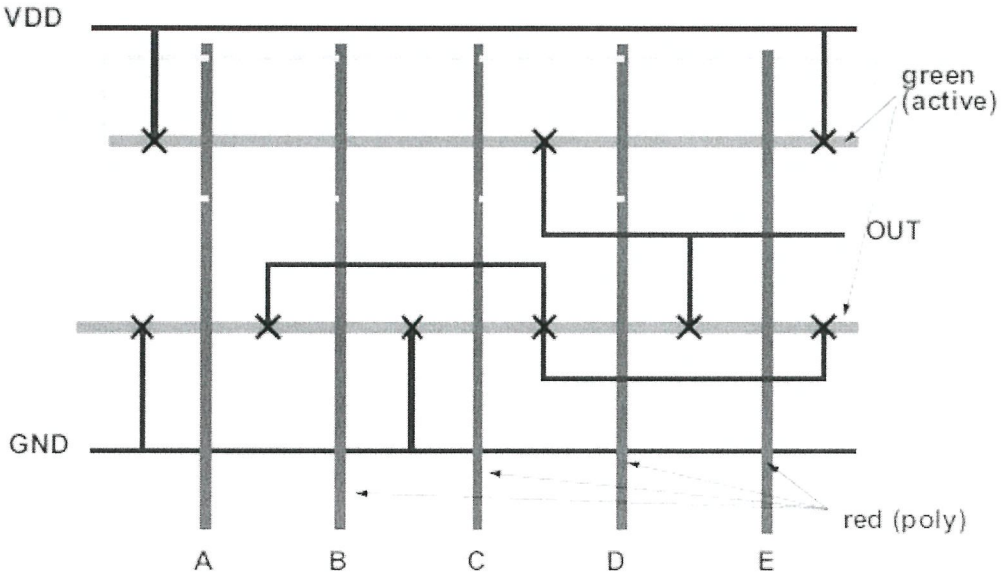

Figure Q1(d)

Q2 (a) Design a fully complementary static CMOS circuit using minimum number of transistors to realize the following function. The circuit need to have a minimum parasitic delay.

$$Y = \overline{CDE + F(A + B)}$$

(10 marks)

(b) Determine the size of each transistor to be used in the design such that the circuit will have an equivalent driving capability of an inverter. Also calculate the minimum parasitic delay. Assume that the minimum length for the transistor is 2λ and the mobility ratio of electron and holes is 2.

(10 marks)

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(c) Calculate the minimum parasitic delay for the circuit.

(5 marks)

Q3 (a) A block diagram of 1-to-4 demultiplexer is shown in **Figure Q3(a)**.

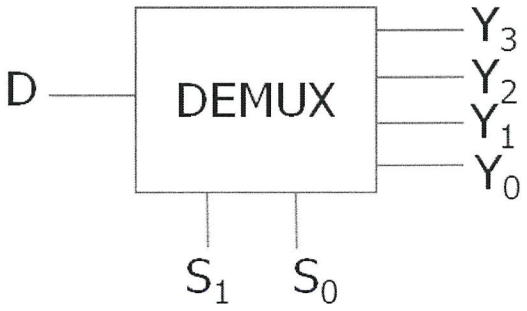

Figure Q3(a)

(i) Establish the truth table for the multiplexer and obtain the equation for each output

(10 marks)

(ii) Design at transistor level using minimum number of transistors the circuit for output Y2 using transmission gate and output Y0 using dynamic logic.

(10 marks)

(b) Compose the Full-Adder circuit at transistor level using transmission gate method to realize the equation for Sum (S) given by:

$$S = A\bar{B}\overline{Cin} + \bar{A}B\overline{Cin} + \bar{A}\bar{B}Cin + ABCin = A \oplus B \oplus Cin$$

(5 marks)

Q4 (a) In sequential circuit, perfect timing is very crucial in determining the correct operation of the circuit. Explain the following timing parameters and illustrate the timing diagram that depict those parameters.

(i) Setup Time

(4 marks)

(ii) Output Delay Time

(4 marks)

(b) **Figure Q4(b)** shows the level sensitive latch circuit. Determine the type of the latch and obtain the equation for the output of the circuit, Q.

(6 marks)

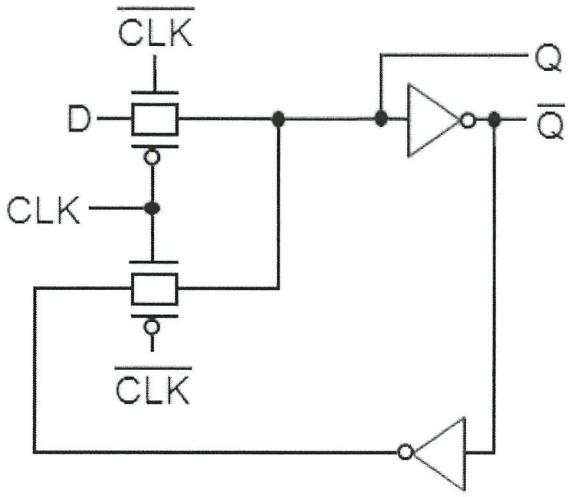

Figure Q4(b)

(c) Analyse the circuit and determine when the circuit is in 'transparent' form and 'opaque' form with regards to the clock input. Assess the output at these two forms.
(6 marks)

(d) Modify the circuit in Figure Q4(b) to produce an opposite level sensitive latch. Draw and clearly label the new circuit and state the new equation for the output.
(5 marks)

- END OF QUESTIONS -