UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2018/2019

COURSE NAME	:	COMPUTER ARCHITECTURE AND ORGANIZATION
COURSE CODE	:	BEC30303
PROGRAMME CODE	:	BEJ
EXAMINATION DATE	:	DECEMBER 2018/ JANUARY 2019
DURATION	:	3 HOURS
INSTRUCTION	:	ANSWER ALL QUESTION IN **SECTION A IN OMR SHEET** AND ALL QUESTIONS IN **SECTION B IN THE QUESTION BOOKLET**

THIS QUESTION PAPER CONSISTS OF **THIRTEEN (13)** PAGES

SECTION A (OBJECTIVE QUESTIONS)

Q1 CPU does not perform the operation _____
a) Data transfer
b) Logic Operation
c) Arithmetic Operation
d) All of the mentioned

(0.5 mark)

Q2 The instruction, Add LOCA, R0 does _____
a) Adds the values of both LOCA and R0 and stores it in R0
b) Adds the value of LOCA to R0 and stores in the temp register
c) Adds the value of R0 to the address of LOCA
d) Adds the value of LOCA with a value in accumulator and stores it in R0

(0.5 mark)

Q3 The primary function of the BUS is
a) To connect the various devices to the CPU
b) To provide a path for communication between the processor and other devices
c) To facilitate data transfer between various devices
d) All of the mentioned

(0.5 mark)

Q4 The two facilities provided by the debugger is
a) Trace points
b) Break points
c) Compile
d) Both Trace and Break points

(0.5 mark)

Q5 In trace mode of operation is _____
a) The program will not be stopped and the errors are sorted out after the complete program is scanned
b) There is no effect on the program, i.e the program is executed without rectification of errors
c) The program is alted only at specific points
d) The program is interrupted after each detection

(0.5 mark)

Q6 A given memory chip has 12 address pins and 4 data pins. It has the following number of locations.
a) 2^4
b) 2^8
c) 2^{10}
d) 2^{12}

(0.5 mark)

Q7 The most important objective of the Universal Serial Bus (USB) is to provide _____

i. Asynchronous data transfer
ii. Easy device connection
iii. Isochronous transmission
iv. Plug and play

a) i, ii, and iii
b) i, ii, and iv
c) i, iii, and iv
d) ii, iii, and iv

(0.5 mark)

Q8 Interrupts can be generated in response to

a) Detected arithmetic overflow error
b) Input output activities
c) Memory activities
d) All of the mentioned

(0.5 mark)

Q9 An interface that provides a method for transferring binary information between internal storage and external devices is called_____

a) I/O interface
b) Memory interface
c) Bus interface
d) Data interface

(0.5 mark)

Q10 The device which starts data transfer is called

a) Initiator
b) Master
c) Transactor
d) Distributor

Q11 _____ register keeps tracks of the instructions stored in program stored in memory.

a) AR (Address Register)
b) PC (Program Counter)
c) XR (Index Register)
d) AC (Accumulator)

(0.5 mark)

Q12 The aim of virtual memory organisation are

i. To provide effective memory access
ii. To provide better memory transfer
iii. To improve the execution of the program

a) i and ii
b) i and iii
c) ii and iii
d) i, ii and iii

(0.5 mark)

Q13 The time between the recieval of an interrupt and its service is _____
a) Trace mode delay
b) Interrupt latency
c) Cycle time
d) Switching time

(0.5 mark)

Q14 Interrupts form an important part of _____ systems.
a) Batch processing
b) Memory
c) Real-time processing
d) Multi-user

(0.5 mark)

Q15 The return address from the interrupt-service routine is stored on the
a) System heap
b) Register
c) Processor stack
d) Memory

(0.5 mark)

Q16 Cache memory acts between_____
a) CPU and RAM
b) RAM and ROM
c) CPU and Hard Disk
d) Primary Storage and Secondary Storage

(0.5 mark)

Q17 Part of the operating system is usually stored in ROM so that it can be used to boot up the computer. ROM is used rather than RAM because
a) ROM chips are faster than RAM
b) ROM chips are not volatile
c) ROM chips are cheaper than RAM chips
d) None of the mentioned

(0.5 mark)

Q18 The effectiveness of the cache memory is based on the property of _____
a) Memory size
b) Locality of reference
c) Memory localization
d) None of the mentioned

(0.5 mark)

Q19 If a magnetic disc has 100 cylinders, each containing 10 tracks of 10 sectors, and each sector can contain 128 bytes, what is the maximum capacity of the disk in bytes?
a) 128
b) 1280
c) 12800
d) 1280000

(0.5 mark)

Q20 PROM stands for _____
a) Pre-fed Read Only Memory
b) Pre-required Read Only Memory
c) Programmed Read Only Memory
d) Programmable Read Only Memory

(0.5 mark)

Q21 The PROM is more effective than ROM chips in regard to _____
a) Cost
b) Memory management
c) Speed of operation
d) Both Cost and Speed of operation

(0.5 mark)

Q22 The memory devices which are similar to EEPROM but differ in the cost effectiveness is _____
a) Memory sticks
b) Blue-ray devices
c) CMOS
d) Flash memory

(0.5 mark)

Q23 An interface that provides I/O transfer of data directly to and form the memory unit and peripheral is termed as
a) DDA
b) DMA
c) Serial Interface
d) Serial Bus

(0.5 mark)

Q24 The average number of steps taken to execute the set of instructions can be made to be less than one by _____
a) ISA
b) Super Scaling
c) Non-pipeline
d) Sequential

(0.5 mark)

Q25 _____ have been developed specifically for pipelined systems.
a) Utility softwares
b) Optimizing compilers
c) Speed up utilities
d) None of the mentioned

(0.5 mark)

Q26 The fetch and execution cycles are interleaved with the help of _____
a) Modification in processor architecture
b) Clock
c) Special unit
d) Control unit

(0.5 mark)

Q27 If a processor clock is rated as 1250 million cycles per second, then its clock period is _____

a) 1.9 x 10-10 sec
b) 1.6 x 10-9 sec
c) 1.25 x 10-10 sec
d) 8 x 10-10 sec

(0.5 mark)

Q28 For a given FINITE number of instructions to be executed, which architecture of the processor provides the fastest execution?

a) ISA
b) Pipeline
c) Non-pipeline
d) Super-scalar

(0.5 mark)

Q29 An application that needed _____ storage alone might not benefit from a cloud deployment at all.

a) online
b) offline
c) virtual
d) None of the mentioned

(0.5 mark)

Q30 _____ describes a distribution model in which applications are hosted by a service provider and made available to users.

a) Infrastructure-as-a-Service (IaaS)
b) Software-as-a-Service (SaaS)
c) Platform-as-a-Service (PaaS)
d) Cloud service

(0.5 mark)

SECTION B (SUBJECTIVE QUESTIONS)

Q31 There are two microprocessors with different instruction format. Each microprocessor requires different amount of time to fetch, decode, execute and store each instruction as shown in **Table Q31.**

Table Q31

Microprocessor	Instruction Type	Time per instruction
CPU X	Two-address format RISC	50 ns
CPU Y	One-address format CISC	40 ns

Assume that the postfix expression needed to be executed is:

$$\boldsymbol{Z = ABC + * D *}$$

(a) Produce the Infix expression of the given operation.

(2 marks)

(5 marks)

(c) Construct instruction set for expression in **Q31** using the one address format CISC.

(5 marks)

(d) Evaluate which microprocessor perform the faster execution time.

(3 marks)

Q32 (a) In accessing the Input and Output devices, there is a need to have a synchronization. Explain the necessity of Input Output device synchronization.

(1 mark)

(b) Briefly explain three possible device synchronization methods.

(6 marks)

(c) In order to instruct the devices, I/O command is needed. Derive four steps in giving I/O command to devices.

(8 marks)

Q33 (a) Compare the control signal approaches in terms of the advantages and disadvantages.

Hardwired Control	Microprogrammed Control

(4 marks)

(b) Based on the block diagram shown in **Figure Q33(b)**, write the step by step the Register Transfer Notation (RTN) to execute the following instruction. Assume that the memory size is 16 bit.

MUL R22, R33

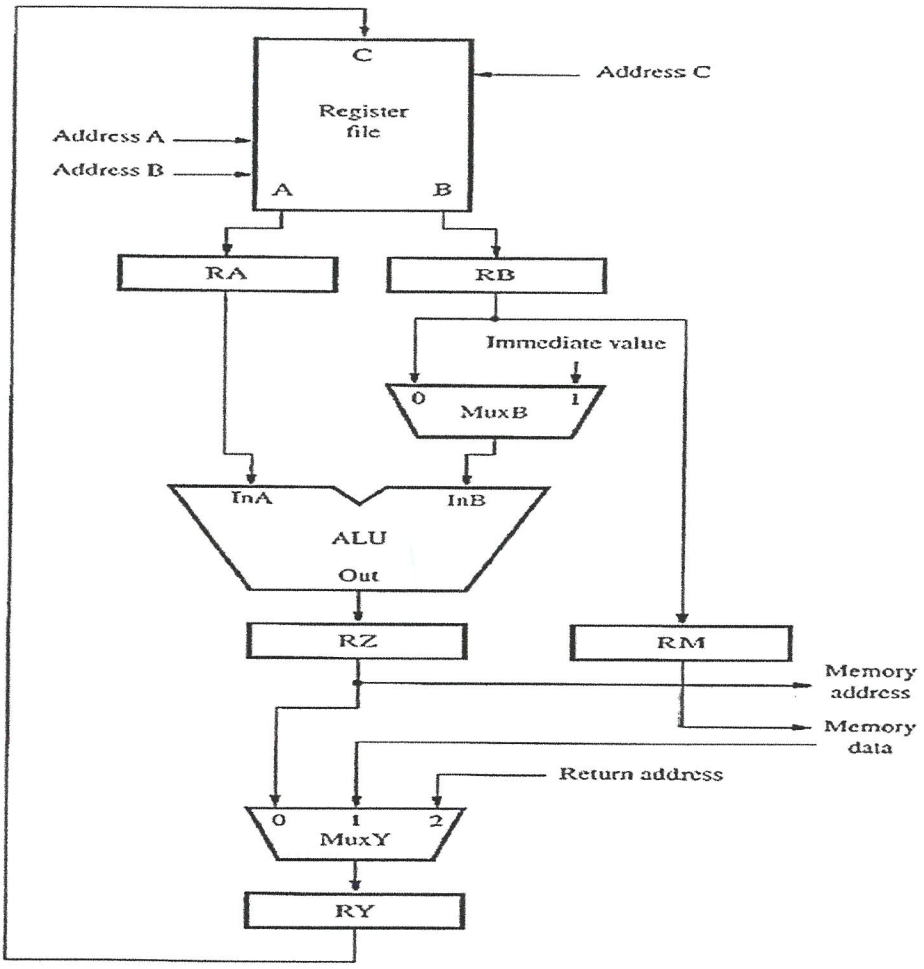

Figure Q33(b)

(11 marks)

Q34 (a) Compare three (3) major differences between SRAM and DRAM.

	SRAM	DRAM
Volatile capability		
Advantage		
Disadvantage		

(6 marks)

(b) Consider a Direct Mapped Cache with features as in **Table Q34(b),** determine the:

Table Q34(b)

Item	Value
Total Number of Cache accessed by CPU	10 access
Total Number of Hit	8 access
Hit Time	4 ns
Miss Penalty	100 ns

(i) Hit rate of the system

(2 marks)

(ii) Miss Rate of the system

(2 marks)

(iii) Average Memory Access Time of the system

(2 marks)

(c) If the cache in **Q34(b)** is replaced with new cache with performance of 97% hit rate and 5 ns hit time, calculate the new Average Memory Access Time for this system.

(3 marks)

Q35 An instruction cycle comprises 4 steps; fetch (F), decode (D), execute (E), and write back (W), where all steps require 1 clock cycle except the execute step, which takes 2 clock cycles. Assume 1 clock cycle = 10 ns.

(a) Sketch the space time diagram to execute five (5) instructions.

(5 marks)

(b) Executing the instruction as in **Q35(a)** may produce Hazard. List 2 (two) possible solution to overcome the problem.

(2 marks)

(c) Calculate the total execution time needed by the pipelined computer to execute a C++ program having 3000 instructions.

(4 marks)

(d) Calculate the performance speed up of the pipelined computer over non-pipelined computer to execute similar C++ program in **Q35(c).**

(4 marks)

Q36 'Cloud Computing' is a technology that offers storage and data access over the Internet from a remote location or computer.

(a) Differentiate between Public and Private types of 'Cloud Computing'.

(2 marks)

(b) 'Cloud Computing' has grown tremendously and obtain huge attention from international company. Justify why this technology is well accepted.

(8 marks)

- **END OF QUESTIONS** -