

**CONFIDENTIAL**



**UNIVERSITI TUN HUSSEIN ONN MALAYSIA**

**FINAL EXAMINATION  
SEMESTER I  
SESSION 2018/2019**

COURSE NAME : MICROPROCESSOR AND  
MICROCONTROLLER

COURSE CODE : BEC30403

PROGRAMME CODE : BEJ

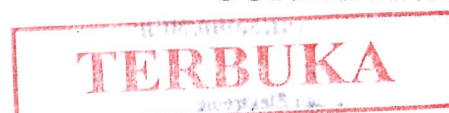
EXAMINATION DATE : DECEMBER 2018 / JANUARY 2019

DURATION : 3 HOURS

INSTRUCTION : ANSWER ALL QUESTIONS

**THIS QUESTION PAPER CONSISTS OF TWENTY (20) PAGES**

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- Q1** (a) List **two (2)** items inside CPU. (2 marks)
- (b) Explain the RLF instruction operation using suitable diagram. (3 marks)
- (c) **Three (3)** buttons function as switches connected to RB0 until RB2 produces an output at LEDs as shown in **Table Q1(c)**. Write a full program for this application. Logic **one (1)** at the switch means pressed, while logic **one (1)** at LED means light up.

**Table Q1(c)**

Switches			LEDs (output)							
RB2	RB1	RB0	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0
0	0	1	0	0	0	1	1	1	1	1
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	1	0	0	0	0	1
1	0	0	0	0	1	0	0	0	1	0
1	0	1	0	0	1	0	0	0	1	1
1	1	0	0	0	1	0	0	1	0	0
1	1	1	0	0	1	0	0	1	0	1

(10 marks)

- (d) (i) Analyse the program in Figure Q1(d) and define its purpose. PORTB connected to eight (8) LEDs.. (2 marks)
- (ii) Identify the simplest programming code technique to replace the program in **Figure Q1(d)**. (8 marks)

```

LOOP MOV LW B'00000010'
MOV WF PORTB

MOV LW B'00000100'
MOV WF PORTB

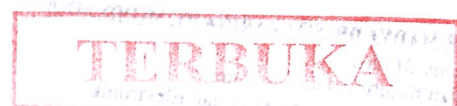
MOV LW B'00000110'
MOV WF PORTB

MOV LW B'00001000'
MOV WF PORTB

MOV LW B'00001010'
MOV WF PORTB

MOV LW B'00001100'
MOV WF PORTB
GOTO LOOP
    
```

**Figure Q1(d)**



**Q2** (a) (i) Define the purpose of **TIMER0**. (2 marks)

(ii) Explain how the **TIMER0** could make **TMROIF** become **one (1)**. (3 marks)

(b) Determine the time that would be taken for the **TIMER0** to count from zero to zero again if crystal 20 MHz and prescaler equal to 8 are used in the calculation. (5 marks)

(c) An engineer in **ASCON Sdn. Bhd.** want to make a new system to monitor a temperature in a room. If the temperature is below 20 °C, the air conditioning system will turn off. If the temperature is between 24 until 20 °C the air conditioning system is off and the normal fan will operate, while when the temperature is above 24 °C, the air conditioning system will be activated. **Table Q2 (c)** shows the system operations.

(i) Write the full program for this application without using interrupt feature.

**Table Q2 (c)**

Temperature (degree) Sensor (RA0)	Air conditioning system status (RA1)	Fan system (RD1)
<20 °C	Turn OFF	
>24 °C	Turn ON	
Between 20 °C and 24 °C		Turn ON
Temperature sensor specification: 40 °C equal to 5V		

(ii) Suggest an improved program applying interrupt for the same application. (10 marks)

(i) List **five (5)** pins in **LCD**. (5 marks)

**Q3** (a) (i) Explain the **five (5)** pins function briefly. (5 marks)

(ii) Calculate the **PWM** duty cycle based on the program shown in **Figure Q3(b)**. Assume that crystal oscillator used is 40 MHz. (5 marks)

(b) (i) Calculate the **PWM** duty cycle based on the program shown in **Figure Q3(b)**. Assume that crystal oscillator used is 40 MHz.

	ORG	000H
	BSF	STATUS, RP0
	MOVLW	B'00000011'
	IORWF	TRISB
	BCF	TRISC,2
	MOVLW	D'249'
	MOVWF	PR2
	BCF	STATUS, RP0
NORMAL	MOVLW	D'220'
	MOVWF	CCPR1L
	MOVLW	B'00000100'
	MOVWF	T2CON
	MOVLW	B'00011100'
	MOVWF	CCP1CON

**Figure Q3(b)(i)**

(4 marks)

(ii) Prove that the PR2 should be inserted with decimal 249 value if the PWM frequency used is 40 KHz.

(3 marks)

(iii) Analyse the program in **Figure Q3(b)(iii)** which using the same criteria in **Q3(b)(i)**. RB0 and RB1 are connected to the buttons.

(3 marks)

MAIN	BTFSS	PORTB,0
	CALL	SPEED1
	BTFSS	PORTB,1
	CALL	SPEED2
	GOTO	MAIN
SPEED1	MOVLW	D'100'
	MOVWF	CCPR1L
	RETURN	
SPEED2	MOVLW	D'50'
	MOVWF	CCPR1L
	RETURN	
	END	

**Figure Q3(b)(iii)**

(iv) Give your conclusion on both speed by calculating the PWM duty cycle.

(5 marks)

- Q4** (a) Differentiate between RAM and ROM. (3 marks)
- (b) Explain the relation of Code Segment register at Bus Interface Unit (BIU) and Code segment area at memory block using a suitable diagram. (5 marks)
- (c) Write a sequence of instructions to add the values from memory location 10100h to 10105h and store the result in AL. (7 marks)
- (d) Modify the codes in **Q4(c)** to use indirect addressing mode. (10 marks)

– END OF QUESTIONS –



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**SPECIAL FUNCTION REGISTER SUMMARY**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on page:	
<b>Bank 0</b>												
00h <sup>(3)</sup>	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)									0000 0000	31, 150
01h	TMR0	Timer0 Module Register									xxxx xxxx	55, 150
02h <sup>(3)</sup>	PCL	Program Counter (PC) Least Significant Byte									0000 0000	30, 150
03h <sup>(3)</sup>	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	22, 150	
04h <sup>(3)</sup>	FSR	Indirect Data Memory Address Pointer									xxxx xxxx	31, 150
05h	PORTA	—	—	PORTA Data Latch when written: PORTA pins when read							--0x 0000	43, 150
06h	PORTB	PORTB Data Latch when written: PORTB pins when read									xxxx xxxx	45, 150
07h	PORTC	PORTC Data Latch when written: PORTC pins when read									xxxx xxxx	47, 150
08h <sup>(4)</sup>	PORTD	PORTD Data Latch when written: PORTD pins when read									xxxx xxxx	48, 150
09h <sup>(4)</sup>	PORTE	—	—	—	—	—	RE2	RE1	RE0	---- -xxx	49, 150	
0Ah <sup>(1,3)</sup>	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	30, 150	
0Bh <sup>(3)</sup>	INTCON	GIE	PEIE	TMROIE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	24, 150	
0Ch	PIR1	PSPIF <sup>(3)</sup>	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	26, 150	
0Dh	PIR2	—	CMIF	—	EEIF	BCLIF	—	—	CCP2IF	-0-0 0--0	28, 150	
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register									xxxx xxxx	60, 150
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register									xxxx xxxx	60, 150
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	--00 0000	57, 150	
11h	TMR2	Timer2 Module Register									0000 0000	62, 150
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	61, 150	
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register									xxxx xxxx	79, 150
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	82, 82, 150	
15h	CCPR1L	Capture/Compare/PWM Register 1 (LSB)									xxxx xxxx	63, 150
16h	CCPR1H	Capture/Compare/PWM Register 1 (MSB)									xxxx xxxx	63, 150
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	64, 150	
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	112, 150	
19h	TXREG	USART Transmit Data Register									0000 0000	118, 150
1Ah	RCREG	USART Receive Data Register									0000 0000	118, 150
1Bh	CCPR2L	Capture/Compare/PWM Register 2 (LSB)									xxxx xxxx	63, 150
1Ch	CCPR2H	Capture/Compare/PWM Register 2 (MSB)									xxxx xxxx	63, 150
1Dh	CCP2CON	—	—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	64, 150	
1Eh	ADRESH	A/D Result Register High Byte									xxxx xxxx	133, 150
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	—	ADON	0000 00-0	127, 150	

**Legend:** x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.  
 Shaded locations are unimplemented, read as '0'.

**Note 1:** The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8>, whose contents are transferred to the upper byte of the program counter.

**2:** Bits PSPIE and PSPIF are reserved on PIC16F873A/876A devices; always maintain these bits clear.

**3:** These registers can be addressed from any bank.

**4:** PORTD, PORTE, TRISD and TRISE are not implemented on PIC16F873A/876A devices, read as '0'.

**5:** Bit 4 of EEADRH implemented only on the PIC16F876A/877A devices.



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**SPECIAL FUNCTION REGISTER SUMMARY (Continued)**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on page:	
<b>Bank 1</b>												
80h <sup>(3)</sup>	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)									0000 0000	31, 150
81h	OPTION_REG	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	23, 150	
82h <sup>(3)</sup>	PCL	Program Counter (PC) Least Significant Byte									0000 0000	30, 150
83h <sup>(3)</sup>	STATUS	IRP	RP1	RP0	T0	PD	Z	DC	C	0001 1xxxx	22, 150	
84h <sup>(3)</sup>	FSR	Indirect Data Memory Address Pointer									xxxxx xxxxx	31, 150
85h	TRISA	—	—	PORTA Data Direction Register						—11 1111	43, 150	
86h	TRISB	PORTB Data Direction Register									1111 1111	45, 150
87h	TRISC	PORTC Data Direction Register									1111 1111	47, 150
88h <sup>(4)</sup>	TRISD	PORTD Data Direction Register									1111 1111	48, 151
89h <sup>(4)</sup>	TRISE	IBF	OBF	IBOV	PSPMODE	—	PORTE Data Direction bits				0000 -111	50, 151
8Ah <sup>(1,3)</sup>	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter						---0 0000	30, 150
8Bh <sup>(3)</sup>	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	24, 150	
8Ch	PIE1	PSPIE <sup>(2)</sup>	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	25, 151	
8Dh	PIE2	—	CMIE	—	EEIE	BCLIE	—	—	CCP2IE	-0-0 0--0	27, 151	
8Eh	PCON	—	—	—	—	—	—	POR	BOR	---- -ggg	29, 151	
8Fh	—	Unimplemented									—	—
90h	—	Unimplemented									—	—
91h	SSPCON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0000 0000	83, 151	
92h	PR2	Timer2 Period Register									1111 1111	62, 151
93h	SSPADDD	Synchronous Serial Port (I <sup>2</sup> C mode) Address Register									0000 0000	79, 151
94h	SSPSTAT	SMP	CKE	D/A	P	S	R/W	UA	BF	0000 0000	79, 151	
95h	—	Unimplemented									—	—
96h	—	Unimplemented									—	—
97h	—	Unimplemented									—	—
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	111, 151	
99h	SPBRG	Baud Rate Generator Register									0000 0000	113, 151
9Ah	—	Unimplemented									—	—
9Bh	—	Unimplemented									—	—
9Ch	CMCON	C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0111	135, 151	
9Dh	CVRCON	CVREN	CVROE	CVRR	—	CVR3	CVR2	CVR1	CVR0	000- 0000	141, 151	
9Eh	ADRESL	A/D Result Register Low Byte									xxxxx xxxxx	133, 151
9Fh	ADCON1	ADFM	ADCS2	—	—	PCFG3	PCFG2	PCFG1	PCFG0	00-- 0000	128, 151	



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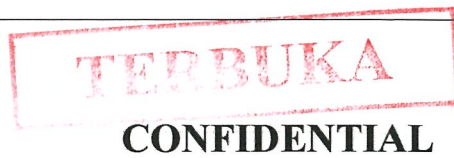
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**SPECIAL FUNCTION REGISTER SUMMARY (Continued)**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on page:	
<b>Bank 2</b>												
100h <sup>(3)</sup>	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)									0000 0000	31, 150
101h	TMR0	Timer0 Module Register									xxxx xxxx	55, 150
102h <sup>(3)</sup>	PCL	Program Counter's (PC) Least Significant Byte									0000 0000	30, 150
103h <sup>(3)</sup>	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxxx	22, 150	
104h <sup>(3)</sup>	FSR	Indirect Data Memory Address Pointer									xxxx xxxx	31, 150
105h	—	Unimplemented									—	—
106h	PORTB	PORTB Data Latch when written: PORTB pins when read									xxxx xxxx	45, 150
107h	—	Unimplemented									—	—
108h	—	Unimplemented									—	—
109h	—	Unimplemented									—	—
10Ah <sup>(1,3)</sup>	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter						---0 0000	30, 150
10Bh <sup>(3)</sup>	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	24, 150	
10Ch	EEDATA	EEPROM Data Register Low Byte									xxxx xxxx	39, 151
10Dh	EEADR	EEPROM Address Register Low Byte									xxxx xxxx	39, 151
10Eh	EEDATH	—	—	EEPROM Data Register High Byte						--xx xxxx	39, 151	
10Fh	EEADRH	—	—	—	— <sup>(5)</sup>	EEPROM Address Register High Byte					---- xxxx	39, 151
<b>Bank 3</b>												
180h <sup>(3)</sup>	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)									0000 0000	31, 150
181h	OPTION_REG	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	23, 150	
182h <sup>(3)</sup>	PCL	Program Counter (PC) Least Significant Byte									0000 0000	30, 150
183h <sup>(3)</sup>	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxxx	22, 150	
184h <sup>(3)</sup>	FSR	Indirect Data Memory Address Pointer									xxxx xxxx	31, 150
185h	—	Unimplemented									—	—
186h	TRISB	PORTB Data Direction Register									1111 1111	45, 150
187h	—	Unimplemented									—	—
188h	—	Unimplemented									—	—
189h	—	Unimplemented									—	—
18Ah <sup>(1,3)</sup>	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter						---0 0000	30, 150
18Bh <sup>(3)</sup>	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	24, 150	
18Ch	EECON1	EEPGD	—	—	—	WRERR	WREN	WR	RD	x--- x000	34, 151	
18Dh	EECON2	EEPROM Control Register 2 (not a physical register)									---- ----	39, 151
18Eh	—	Reserved; maintain clear									0000 0000	—
18Fh	—	Reserved; maintain clear									0000 0000	—

- Legend:** x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.  
 Shaded locations are unimplemented, read as '0'.
- Note** 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8>, whose contents are transferred to the upper byte of the program counter.  
 2: Bits PSPIE and PSPIF are reserved on PIC16F873A/876A devices; always maintain these bits clear.  
 3: These registers can be addressed from any bank.  
 4: PORTD, PORTE, TRISD and TRISE are not implemented on PIC16F873A/876A devices, read as '0'.  
 5: Bit 4 of EEADRH implemented only on the PIC16F876A/877A devices.



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**STATUS REGISTER (ADDRESS 03h, 83h, 103h, 183h)**

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C

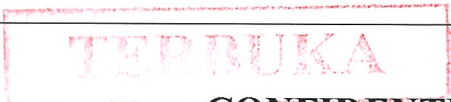
bit 7

bit 0

- bit 7 **IRP:** Register Bank Select bit (used for indirect addressing)  
 1 = Bank 2, 3 (100h-1FFh)  
 0 = Bank 0, 1 (00h-FFh)
- bit 6-5 **RP1:RP0:** Register Bank Select bits (used for direct addressing)  
 11 = Bank 3 (180h-1FFh)  
 10 = Bank 2 (100h-17Fh)  
 01 = Bank 1 (80h-FFh)  
 00 = Bank 0 (00h-7Fh)  
 Each bank is 128 bytes.
- bit 4  **$\overline{TO}$ :** Time-out bit  
 1 = After power-up, CLRWDT instruction or SLEEP instruction  
 0 = A WDT time-out occurred
- bit 3  **$\overline{PD}$ :** Power-down bit  
 1 = After power-up or by the CLRWDT instruction  
 0 = By execution of the SLEEP instruction
- bit 2 **Z:** Zero bit  
 1 = The result of an arithmetic or logic operation is zero  
 0 = The result of an arithmetic or logic operation is not zero
- bit 1 **DC:** Digit carry/borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)  
 (for borrow, the polarity is reversed)  
 1 = A carry-out from the 4th low order bit of the result occurred  
 0 = No carry-out from the 4th low order bit of the result
- bit 0 **C:** Carry/borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)  
 1 = A carry-out from the Most Significant bit of the result occurred  
 0 = No carry-out from the Most Significant bit of the result occurred

**Note:** For borrow, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high, or low order bit of the source register.

<b>Legend:</b>			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown



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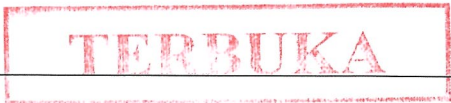
**OPTION\_REG REGISTER (ADDRESS 81h, 181h)**

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
RBP $\bar{U}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

- bit 7 **RBP $\bar{U}$** : PORTB Pull-up Enable bit  
 1 = PORTB pull-ups are disabled  
 0 = PORTB pull-ups are enabled by individual port latch values
- bit 6 **INTEDG**: Interrupt Edge Select bit  
 1 = Interrupt on rising edge of RB0/INT pin  
 0 = Interrupt on falling edge of RB0/INT pin
- bit 5 **T0CS**: TMR0 Clock Source Select bit  
 1 = Transition on RA4/T0CKI pin  
 0 = Internal instruction cycle clock (CLKO)
- bit 4 **T0SE**: TMR0 Source Edge Select bit  
 1 = Increment on high-to-low transition on RA4/T0CKI pin  
 0 = Increment on low-to-high transition on RA4/T0CKI pin
- bit 3 **PSA**: Prescaler Assignment bit  
 1 = Prescaler is assigned to the WDT  
 0 = Prescaler is assigned to the Timer0 module
- bit 2-0 **PS2:PS0**: Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

**Legend:**  
 R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 - n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown



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**INTCON REGISTER (ADDRESS 0Bh, 8Bh, 10Bh, 18Bh)**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF
bit 7						bit 0	

- bit 7 **GIE:** Global Interrupt Enable bit  
 1 = Enables all unmasked interrupts  
 0 = Disables all interrupts
- bit 6 **PEIE:** Peripheral Interrupt Enable bit  
 1 = Enables all unmasked peripheral interrupts  
 0 = Disables all peripheral interrupts
- bit 5 **TMR0IE:** TMR0 Overflow Interrupt Enable bit  
 1 = Enables the TMR0 interrupt  
 0 = Disables the TMR0 interrupt
- bit 4 **INTE:** RB0/INT External Interrupt Enable bit  
 1 = Enables the RB0/INT external interrupt  
 0 = Disables the RB0/INT external interrupt
- bit 3 **RBIE:** RB Port Change Interrupt Enable bit  
 1 = Enables the RB port change interrupt  
 0 = Disables the RB port change interrupt
- bit 2 **TMR0IF:** TMR0 Overflow Interrupt Flag bit  
 1 = TMR0 register has overflowed (must be cleared in software)  
 0 = TMR0 register did not overflow
- bit 1 **INTF:** RB0/INT External Interrupt Flag bit  
 1 = The RB0/INT external interrupt occurred (must be cleared in software)  
 0 = The RB0/INT external interrupt did not occur
- bit 0 **RBIF:** RB Port Change Interrupt Flag bit  
 1 = At least one of the RB7:RB4 pins changed state; a mismatch condition will continue to set the bit. Reading PORTB will end the mismatch condition and allow the bit to be cleared (must be cleared in software).  
 0 = None of the RB7:RB4 pins have changed state

<b>Legend:</b>			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown



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**FINAL EXAMINATION**

SEMESTER / SESSION : SEM I / 2018/2019  
 COURSE : MICROPROCESSOR AND MICROCONTROLLER

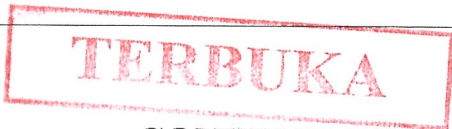
PROGRAMME : BEJ  
 COURSE CODE : BEC30403

**PIE1 REGISTER (ADDRESS 8Ch)**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PSPIE <sup>(1)</sup>	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE
bit 7						bit 0	

- bit 7 **PSPIE:** Parallel Slave Port Read/Write Interrupt Enable bit<sup>(1)</sup>  
 1 = Enables the PSP read/write interrupt  
 0 = Disables the PSP read/write interrupt  
**Note 1:** PSPIE is reserved on PIC16F873A/876A devices; always maintain this bit clear.
- bit 6 **ADIE:** A/D Converter Interrupt Enable bit  
 1 = Enables the A/D converter interrupt  
 0 = Disables the A/D converter interrupt
- bit 5 **RCIE:** USART Receive Interrupt Enable bit  
 1 = Enables the USART receive interrupt  
 0 = Disables the USART receive interrupt
- bit 4 **TXIE:** USART Transmit Interrupt Enable bit  
 1 = Enables the USART transmit interrupt  
 0 = Disables the USART transmit interrupt
- bit 3 **SSPIE:** Synchronous Serial Port Interrupt Enable bit  
 1 = Enables the SSP interrupt  
 0 = Disables the SSP interrupt
- bit 2 **CCP1IE:** CCP1 Interrupt Enable bit  
 1 = Enables the CCP1 interrupt  
 0 = Disables the CCP1 interrupt
- bit 1 **TMR2IE:** TMR2 to PR2 Match Interrupt Enable bit  
 1 = Enables the TMR2 to PR2 match interrupt  
 0 = Disables the TMR2 to PR2 match interrupt
- bit 0 **TMR1IE:** TMR1 Overflow Interrupt Enable bit  
 1 = Enables the TMR1 overflow interrupt  
 0 = Disables the TMR1 overflow interrupt

<b>Legend:</b>			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown



**FINAL EXAMINATION**

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PROGRAMME : BEJ  
 COURSE CODE : BEC30403

**PIR1 REGISTER (ADDRESS 0Ch)**

R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
PSPIF <sup>(1)</sup>	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF
bit 7				bit 0			

- bit 7 **PSPIF**: Parallel Slave Port Read/Write Interrupt Flag bit<sup>(1)</sup>  
 1 = A read or a write operation has taken place (must be cleared in software)  
 0 = No read or write has occurred  
**Note 1:** PSPIF is reserved on PIC16F873A/876A devices; always maintain this bit clear.
- bit 6 **ADIF**: A/D Converter Interrupt Flag bit  
 1 = An A/D conversion completed  
 0 = The A/D conversion is not complete
- bit 5 **RCIF**: USART Receive Interrupt Flag bit  
 1 = The USART receive buffer is full  
 0 = The USART receive buffer is empty
- bit 4 **TXIF**: USART Transmit Interrupt Flag bit  
 1 = The USART transmit buffer is empty  
 0 = The USART transmit buffer is full
- bit 3 **SSPIF**: Synchronous Serial Port (SSP) Interrupt Flag bit  
 1 = The SSP interrupt condition has occurred and must be cleared in software before returning from the Interrupt Service Routine. The conditions that will set this bit are:
  - SPI – A transmission/reception has taken place.
  - I<sup>2</sup>C Slave – A transmission/reception has taken place.
  - I<sup>2</sup>C Master
    - A transmission/reception has taken place.
    - The initiated Start condition was completed by the SSP module.
    - The initiated Stop condition was completed by the SSP module.
    - The initiated Restart condition was completed by the SSP module.
    - The initiated Acknowledge condition was completed by the SSP module.
    - A Start condition occurred while the SSP module was Idle (multi-master system).
    - A Stop condition occurred while the SSP module was Idle (multi-master system).
 0 = No SSP interrupt condition has occurred
- bit 2 **CCP1IF**: CCP1 Interrupt Flag bit  
Capture mode:  
 1 = A TMR1 register capture occurred (must be cleared in software)  
 0 = No TMR1 register capture occurred  
Compare mode:  
 1 = A TMR1 register compare match occurred (must be cleared in software)  
 0 = No TMR1 register compare match occurred  
PWM mode:  
 Unused in this mode.
- bit 1 **TMR2IF**: TMR2 to PR2 Match Interrupt Flag bit  
 1 = TMR2 to PR2 match occurred (must be cleared in software)  
 0 = No TMR2 to PR2 match occurred
- bit 0 **TMR1IF**: TMR1 Overflow Interrupt Flag bit  
 1 = TMR1 register overflowed (must be cleared in software)  
 0 = TMR1 register did not overflow

<b>Legend:</b>			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown



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**FINAL EXAMINATION**

SEMESTER / SESSION : SEM I / 2018/2019  
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PROGRAMME : BEJ  
 COURSE CODE : BEC30403

**REGISTERS ASSOCIATED WITH PWM AND TIMER2**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Bh,8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF <sup>(1)</sup>	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
0Dh	PIR2	—	—	—	—	—	—	—	CCP2IF	---- --0	---- --0
8Ch	PIE1	PSPIE <sup>(1)</sup>	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
8Dh	PIE2	—	—	—	—	—	—	—	CCP2IE	---- --0	---- --0
87h	TRISC	PORTC Data Direction Register								1111 1111	1111 1111
11h	TMR2	Timer2 Module's Register								0000 0000	0000 0000
92h	PR2	Timer2 Module's Period Register								1111 1111	1111 1111
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
15h	CCPR1L	Capture/Compare/PWM Register 1 (LSB)								xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Compare/PWM Register 1 (MSB)								xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
1Bh	CCPR2L	Capture/Compare/PWM Register 2 (LSB)								xxxx xxxx	uuuu uuuu
1Ch	CCPR2H	Capture/Compare/PWM Register 2 (MSB)								xxxx xxxx	uuuu uuuu
1Dh	CCP2CON	—	—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	--00 0000

**Legend:** x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by PWM and Timer2.

**Note 1:** Bits PSPIE and PSPIF are reserved on 28-pin devices; always maintain these bits clear.

**SETUP FOR PWM OPERATION**

The following steps should be taken when configuring the CCP module for PWM operation:

1. Set the PWM period by writing to the PR2 register.
2. Set the PWM duty cycle by writing to the CCPR1L register and CCP1CON<5:4> bits.
3. Make the CCP1 pin an output by clearing the TRISC<2> bit.
4. Set the TMR2 prescale value and enable Timer2 by writing to T2CON.
5. Configure the CCP1 module for PWM operation.

$$\text{PWM Period} = [(PR2) + 1] \cdot 4 \cdot \text{TOSC} \cdot (\text{TMR2 Prescale Value})$$

$$\text{PWM Duty Cycle} = (\text{CCPR1L}:\text{CCP1CON}\langle 5:4 \rangle) \cdot \text{Tosc} \cdot (\text{TMR2 Prescale Value})$$



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**T2CON: TIMER2 CONTROL REGISTER (ADDRESS 12h)**

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0
bit 7							bit 0

- bit 7 **Unimplemented:** Read as '0'
- bit 6-3 **TOUTPS3:TOUTPS0:** Timer2 Output Postscale Select bits
  - 0000 = 1:1 postscale
  - 0001 = 1:2 postscale
  - 0010 = 1:3 postscale
  - .
  - .
  - .
  - 1111 = 1:16 postscale
- bit 2 **TMR2ON:** Timer2 On bit
  - 1 = Timer2 is on
  - 0 = Timer2 is off
- bit 1-0 **T2CKPS1:T2CKPS0:** Timer2 Clock Prescale Select bits
  - 00 = Prescaler is 1
  - 01 = Prescaler is 4
  - 1x = Prescaler is 16

<b>Legend:</b>			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown



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**ADCON0 REGISTER (ADDRESS 1Fh)**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	—	ADON
bit 7						bit 0	

bit 7-6 **ADCS1:ADCS0**: A/D Conversion Clock Select bits (ADCON0 bits in **bold**)

ADCON1 <ADCS2>	ADCON0 <ADCS1:ADCS0>	Clock Conversion
0	<b>00</b>	Fosc/2
0	<b>01</b>	Fosc/8
0	<b>10</b>	Fosc/32
0	<b>11</b>	Frc (clock derived from the internal A/D RC oscillator)
1	<b>00</b>	Fosc/4
1	<b>01</b>	Fosc/16
1	<b>10</b>	Fosc/64
1	<b>11</b>	Frc (clock derived from the internal A/D RC oscillator)

bit 5-3 **CHS2:CHS0**: Analog Channel Select bits

- 000 = Channel 0 (AN0)
- 001 = Channel 1 (AN1)
- 010 = Channel 2 (AN2)
- 011 = Channel 3 (AN3)
- 100 = Channel 4 (AN4)
- 101 = Channel 5 (AN5)
- 110 = Channel 6 (AN6)
- 111 = Channel 7 (AN7)

**Note:** The PIC16F873A/876A devices only implement A/D channels 0 through 4; the unimplemented selections are reserved. Do not select any unimplemented channels with these devices.

bit 2 **GO/DONE**: A/D Conversion Status bit

When **ADON = 1**:

- 1 = A/D conversion in progress (setting this bit starts the A/D conversion which is automatically cleared by hardware when the A/D conversion is complete)
- 0 = A/D conversion not in progress

bit 1 **Unimplemented**: Read as '0'

bit 0 **ADON**: A/D On bit

- 1 = A/D converter module is powered up
- 0 = A/D converter module is shut-off and consumes no operating current

<b>Legend:</b>			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown



**FINAL EXAMINATION**

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PROGRAMME : BEJ  
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**ADCON1 REGISTER (ADDRESS 9Fh)**

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	ADCS2	—	—	PCFG3	PCFG2	PCFG1	PCFG0
bit 7				bit 0			

bit 7 **ADFM**: A/D Result Format Select bit

1 = Right justified. Six (6) Most Significant bits of ADRESH are read as '0'.  
 0 = Left justified. Six (6) Least Significant bits of ADRESL are read as '0'.

bit 6 **ADCS2**: A/D Conversion Clock Select bit (ADCON1 bits in shaded area and in bold)

ADCON1 <ADCS2>	ADCON0 <ADCS1:ADCS0>	Clock Conversion
0	00	Fosc/2
0	01	Fosc/8
0	10	Fosc/32
0	11	FRC (clock derived from the internal A/D RC oscillator)
1	00	Fosc/4
1	01	Fosc/16
1	10	Fosc/64
1	11	FRC (clock derived from the internal A/D RC oscillator)

bit 5-4 **Unimplemented**: Read as '0'

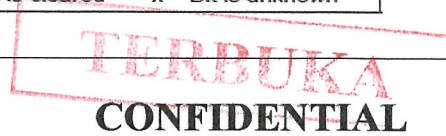
bit 3-0 **PCFG3:PCFG0**: A/D Port Configuration Control bits

PCFG <3:0>	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0	VREF+	VREF-	C/R
0000	A	A	A	A	A	A	A	A	VDD	VSS	8/0
0001	A	A	A	A	VREF+	A	A	A	AN3	VSS	7/1
0010	D	D	D	A	A	A	A	A	VDD	VSS	5/0
0011	D	D	D	A	VREF+	A	A	A	AN3	VSS	4/1
0100	D	D	D	D	A	D	A	A	VDD	VSS	3/0
0101	D	D	D	D	VREF+	D	A	A	AN3	VSS	2/1
011x	D	D	D	D	D	D	D	D	—	—	0/0
1000	A	A	A	A	VREF+	VREF-	A	A	AN3	AN2	6/2
1001	D	D	A	A	A	A	A	A	VDD	VSS	6/0
1010	D	D	A	A	VREF+	A	A	A	AN3	VSS	5/1
1011	D	D	A	A	VREF+	VREF-	A	A	AN3	AN2	4/2
1100	D	D	D	A	VREF+	VREF-	A	A	AN3	AN2	3/2
1101	D	D	D	D	VREF+	VREF-	A	A	AN3	AN2	2/2
1110	D	D	D	D	D	D	D	A	VDD	VSS	1/0
1111	D	D	D	D	VREF+	VREF-	D	A	AN3	AN2	1/2

A = Analog input D = Digital I/O

C/R = # of analog input channels/# of A/D voltage references

<b>Legend:</b>			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown



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PROGRAMME : BEJ  
 COURSE CODE : BEC30403

**REGISTERS/BITS ASSOCIATED WITH A/D**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on MCLR, WDT
0Bh,8Bh,10Bh,18Bh	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF <sup>(1)</sup>	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
8Ch	PIE1	PSPIE <sup>(1)</sup>	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
1Eh	ADRESH	A/D Result Register High Byte								xxxxx xxxxx	uuuu uuuu
9Eh	ADRESL	A/D Result Register Low Byte								xxxxx xxxxx	uuuu uuuu
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	—	ADON	0000 00-0	0000 00-0
9Fh	ADCON1	ADFM	ADCS2	—	—	PCFG3	PCFG2	PCFG1	PCFG0	00-- 0000	00-- 0000
85h	TRISA	—	—	PORTA Data Direction Register						--11 1111	--11 1111
05h	PORTA	—	—	PORTA Data Latch when written: PORTA pins when read						--0x 0000	--0u 0000
89h <sup>(1)</sup>	TRISE	IBF	OBF	IBOV	PSPMODE	—	PORTE Data Direction bits			0000 -111	0000 -111
09h <sup>(1)</sup>	PORTE	—	—	—	—	—	RE2	RE1	RE0	---- -xxxx	---- -uuu

**Legend:** x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used for A/D conversion.  
**Note 1:** These registers are not available on 28-pin devices.

**BAUD RATE FORMULA**

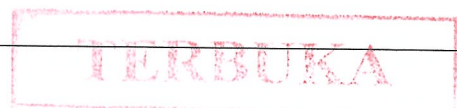
SYNC	BRGH = 0 (Low Speed)	BRGH = 1 (High Speed)
0	(Asynchronous) Baud Rate = $F_{osc}/(64(X+1))$	Baud Rate = $F_{osc}/(16(X+1))$
1	(Synchronous) Baud Rate = $F_{osc}/(4(X+1))$	N/A

**Legend:** X = value in SPBRG (0 to 255)

**REGISTERS ASSOCIATED WITH BAUD RATE GENERATOR**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

**Legend:** x = unknown, - = unimplemented, read as '0'. Shaded cells are not used by the BRG.



**FINAL EXAMINATION**

SEMESTER / SESSION : SEM I / 2018/2019  
 COURSE : MICROPROCESSOR AND MICROCONTROLLER

PROGRAMME : BEJ  
 COURSE CODE : BEC30403

**Instruction Set Summary**

Mnemonic, Operands	Description	Cycles	14-Bit Opcode		Status Affected	Notes
			MSb	LSb		
<b>BYTE-ORIENTED FILE REGISTER OPERATIONS</b>						
ADDWF	f, d Add W and f	1	00	0111 dfff ffff	C,DC,Z	1,2
ANDWF	f, d AND W with f	1	00	0101 dfff ffff	Z	1,2
CLRF	f Clear f	1	00	0001 lfff ffff	Z	2
CLRWF	- Clear W	1	00	0001 0xxx xxxx	Z	
COMF	f, d Complement f	1	00	1001 dfff ffff	Z	1,2
DECf	f, d Decrement f	1	00	0011 dfff ffff	Z	1,2
DECFSZ	f, d Decrement f, Skip if 0	1(2)	00	1011 dfff ffff		1,2,3
INCF	f, d Increment f	1	00	1010 dfff ffff	Z	1,2
INCFSZ	f, d Increment f, Skip if 0	1(2)	00	1111 dfff ffff		1,2,3
IORWF	f, d Inclusive OR W with f	1	00	0100 dfff ffff	Z	1,2
MOVf	f, d Move f	1	00	1000 dfff ffff	Z	1,2
MOVWF	f Move W to f	1	00	0000 lfff ffff		
NOP	- No Operation	1	00	0000 0xxx 0000		
RLF	f, d Rotate Left f through Carry	1	00	1101 dfff ffff	C	1,2
RRF	f, d Rotate Right f through Carry	1	00	1100 dfff ffff	C	1,2
SUBWF	f, d Subtract W from f	1	00	0010 dfff ffff	C,DC,Z	1,2
SWAPf	f, d Swap nibbles in f	1	00	1110 dfff ffff		1,2
XORWF	f, d Exclusive OR W with f	1	00	0110 dfff ffff	Z	1,2
<b>BIT-ORIENTED FILE REGISTER OPERATIONS</b>						
BCF	f, b Bit Clear f	1	01	00bb bfff ffff		1,2
BSF	f, b Bit Set f	1	01	01bb bfff ffff		1,2
BTFSC	f, b Bit Test f, Skip if Clear	1 (2)	01	10bb bfff ffff		3
BTFSS	f, b Bit Test f, Skip if Set	1 (2)	01	11bb bfff ffff		3
<b>LITERAL AND CONTROL OPERATIONS</b>						
ADDLW	k Add Literal and W	1	11	111x kkkk kkkk	C,DC,Z	
ANDLW	k AND Literal with W	1	11	1001 kkkk kkkk	Z	
CALL	k Call Subroutine	2	10	0kkk kkkk kkkk		
CLRWDt	- Clear Watchdog Timer	1	00	0000 0110 0100	$\overline{TO,PD}$	
GOTO	k Go to Address	2	10	1kkk kkkk kkkk		
IORLW	k Inclusive OR Literal with W	1	11	1000 kkkk kkkk	Z	
MOVLW	k Move Literal to W	1	11	00xx kkkk kkkk		
RETFIE	- Return from Interrupt	2	00	0000 0000 1001		
RETLW	k Return with Literal in W	2	11	01xx kkkk kkkk		
RETURN	- Return from Subroutine	2	00	0000 0000 1000		
SLEEP	- Go into Standby mode	1	00	0000 0110 0011	$\overline{TO,PD}$	
SUBLW	k Subtract W from Literal	1	11	110x kkkk kkkk	C,DC,Z	
XORLW	k Exclusive OR Literal with W	1	11	1010 kkkk kkkk	Z	



TERBUKA