Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2017/2018

COURSE NAME	:	DIGITAL ELECTRONICS
COURSE CODE	:	BEL 20303
PROGRAMME	:	BEV/ BEJ
EXAMINATION DATE	:	JUNE/ JULY 2018
DURATION	:	3 HOURS
INSTRUCTION	:	1. ANSWER **ALL** QUESTIONS IN THIS BOOKLET. 2. **NO CALCULATOR** IS ALLOWED.

THIS QUESTION PAPER CONSISTS OF TWELVE **(12)** PAGES

Q1 (a) Assuming that all numbers can be represented using 8 bit binary, complete the missing entries which are not shaded in the Table **Q1 (a)**. Also assume two's complement numbering system is used where necessary. (No mark will be awarded for this question unless you show how the solutions are derived).

(8 marks)

TABLE Q1(a)

Binary	Hexadecimal	Decimal	BCD	Gray
(i)		81		(ii)
	F4	(iii)	(iv)	

(b) Given the Boolean expression:

$$Y = (a + b + c)(b + c + d)(\bar{a} + \bar{b} + \bar{d})(\bar{b}+\bar{c}+\bar{d})$$

(i) Construct a truth table for output Y

(8 marks)

(ii) Derive the minimal sum-of-product of expression Y using Karnaugh map.

(6 marks)

(iii) Implement the circuit for the simplest Boolean expression.

(3 marks)

Q2 (a) A combinational circuit has three inputs X, Y, and Z. Its output are 2-bit binary number which are F1 and F0. This circuit will counts the number of 1 present in the inputs.

(i) Obtain the truth table for this combinational circuit.

(4 marks)

(ii) Derive the minimal sum-of-product of expression F1 and F0.

(6 marks)

(b) Design a system, which has three inputs (A2, A1 and A0) and produces two outputs, X and Y. The output X is HIGH (1) whenever A2 and A0 are HIGH. Output Y is HIGH when X and A2 are both HIGH OR X and A1 are both LOW (0). Using the logic symbol of IC 74LS138 (3-to-8 line decoder) shown in **Figure Q2(b)**, implement this system together with the external logic gates. Show all the steps and wiring of the IC 74LS138.

(10 marks)

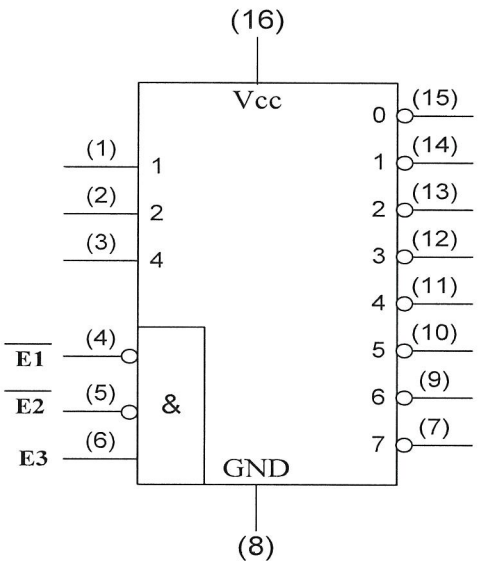

Figure Q2(b)

(c) Show how a 74LS151 IC (8-to-1 multiplexer) in **Figure Q2(c)** is used to implement the function:

$$F = A.B.\bar{C} + \bar{A}.B.C + A.\bar{B}.\bar{C} + A.B.C$$

(5 marks)

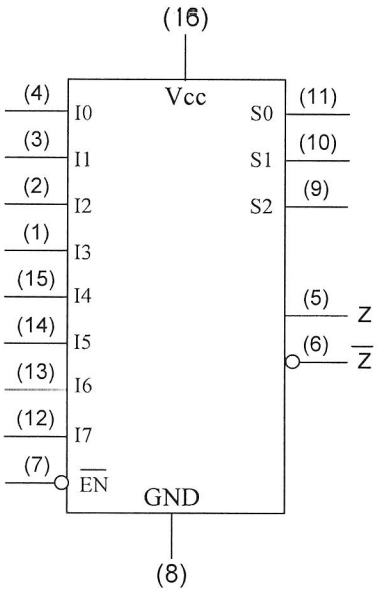

Figure Q2(c)

Q3 (a) Explain the differences in S-R and J-K flip flop.

(4 marks)

(b) **Figure Q3(b)(i)** is a logic circuit that comprises of a JK, SC and D flip-flop. **Figure Q3(b)(ii)** shows the waveforms for signal CLK, X, Y, $\overline{CLR}$ and $\overline{PRE}$. Complete the timing diagram for Q_A, Q_B and Q_C in **Figure Q3(b)(ii)** Assume that Q_A, Q_B and Q_C are at high level initially.

(12 marks)

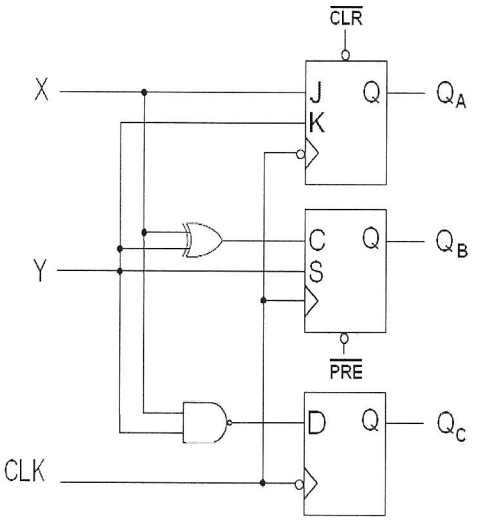

Figure Q3(b)(i)

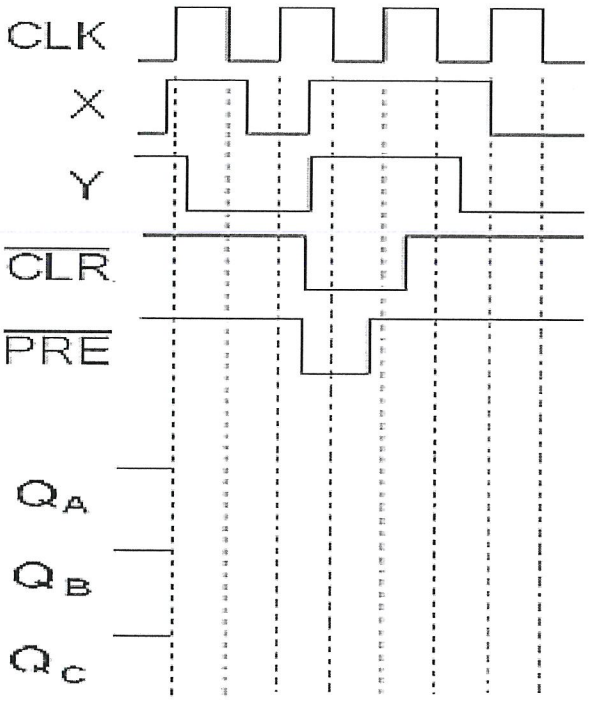

Figure Q3(b)(ii)

(c) Given the circuit diagram in **Figure Q3(c)(i)**, determine the timing diagram for S, C and Q in **Figure Q3(c)(ii)**. Assume that Q is in high state initially.

(9 marks)

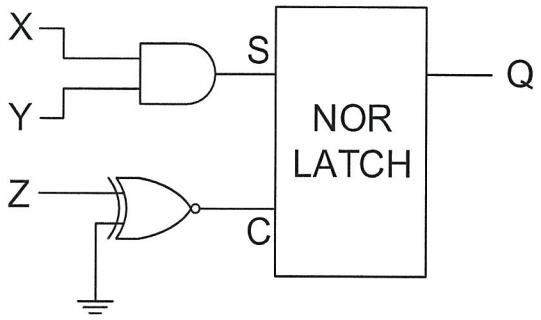

Figure Q3(c)(i)

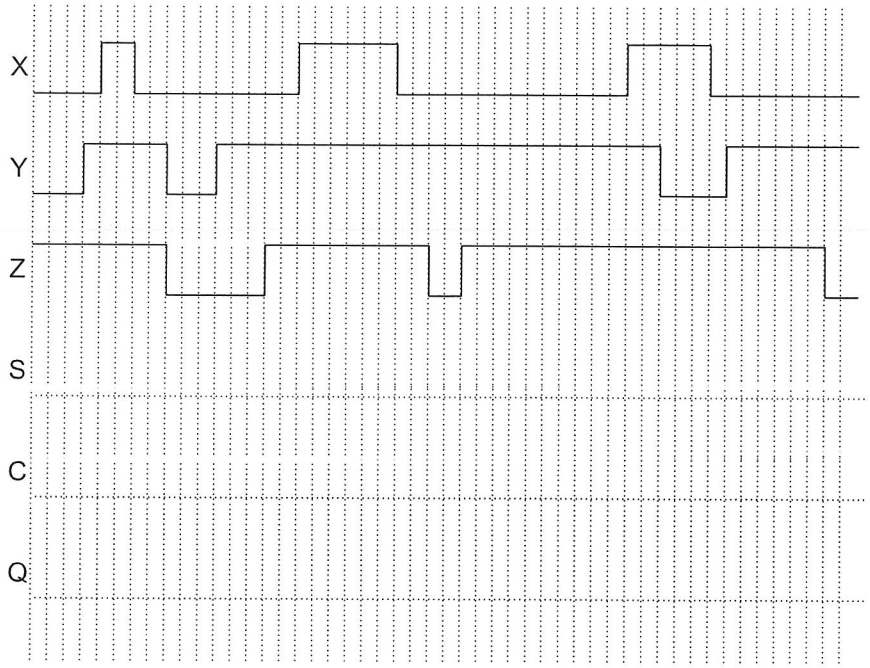

Figure Q3(c)(ii)

Q4 **Figure Q4(a)(i)** shows a register and **Figure Q4(a)(ii)** shows the input waveforms (CLOCK and Data in) to the circuit.

(a) Analyse the circuit and draw the output waveforms for Q_{U1}, Q_{U2}, Q_{U3} and Q_{U4} in **Figure Q4(b)(ii).**

(8 marks)

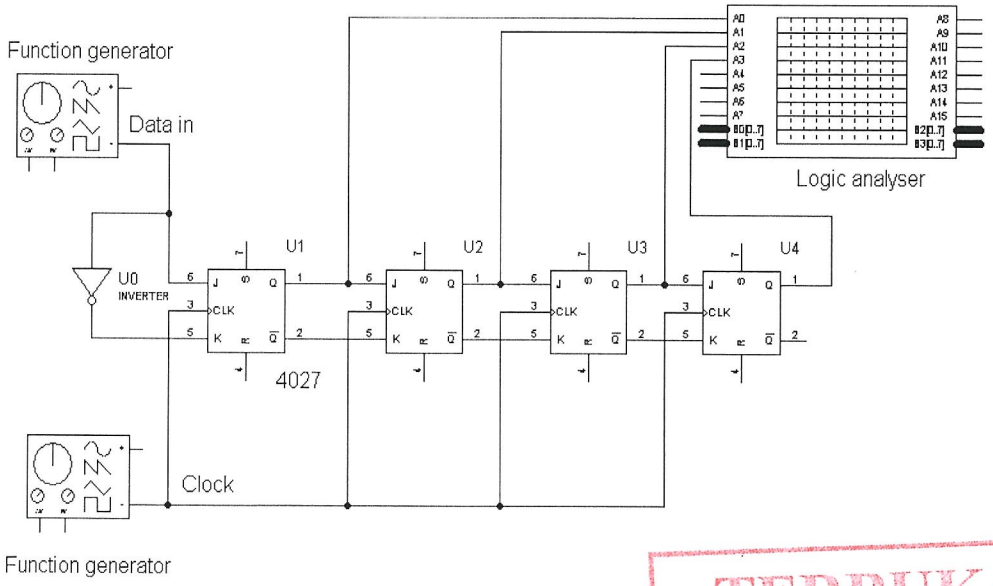

Figure Q4(a)(i)

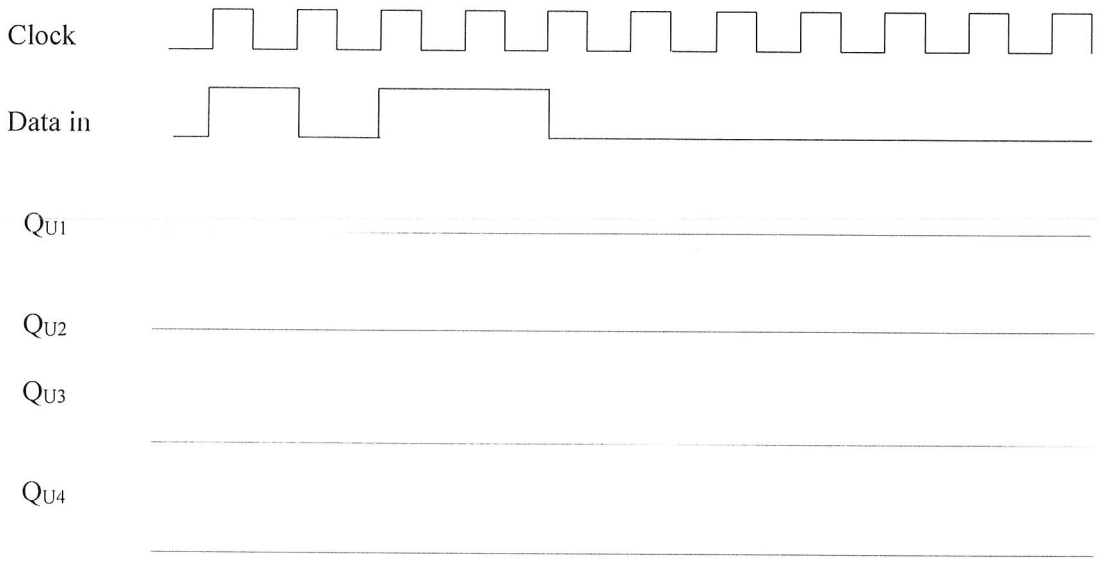

Figure Q4(b)(ii)

a) Analyse and state the type of register as shown in **Figure Q4 (a)(i)**.

(2 marks)

(c) **Figure Q4(c)** shows the state transition diagram of a state machine.

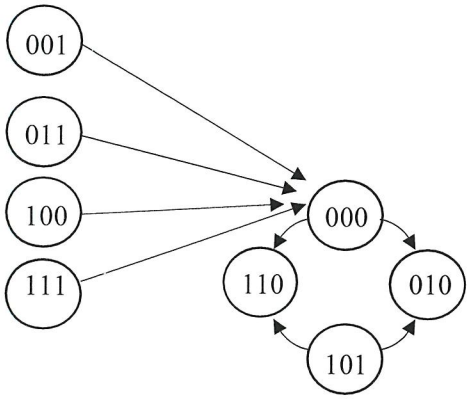

Figure Q4(c)

(i) Build the excitation table for this state machine.

(5 marks)

(ii) Find the simplest Boolean expression for the circuit using Karnaugh map.

(6 marks)

(iii) Implement the circuit diagram

(4 marks)

- END OF QUESTIONS -