Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2017/2018

COURSE NAME	:	DIGITAL DESIGN
COURSE CODE	:	BEC 30503
PROGRAMME CODE	:	BEJ
EXAMINATION DATE	:	JUNE/JULY 2018
DURATION	:	3 HOURS
INSTRUCTION	:	ANSWER **ALL** QUESTIONS

THIS QUESTION PAPER CONSISTS OF **FOUR (4)** PAGES

Q1 (a) Explain the similarities between VHDL and Verilog?

(6 marks)

(b) Sketch and explain the digital design flow for logic circuits.

(10 marks)

(c) Explain the difference betweens Combinational digital circuit and Sequential digital circuit.

(10 marks)

Q2 (a) By referring to the **Table Q2(a)**, construct the PAL logic circuit. The three variables, ***a***, ***b***, and ***c***, are input signals, and the two variables, ***x*** and ***y***, are output signals.

(7 marks)

Table Q2(a) Truth Table

a	*b*	*c*	*x*	*y*
0	0	0	1	0
0	0	1	0	0
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	1
1	1	0	1	0
1	1	1	0	0

(b) List the differences of the hardware properties between FPGAs and microcontrollers.

(5 marks)

(c) Construct a 4-to-1 multiplexer by using a 2-to-4 decoder and other necessary gates.

(4 marks)

Q3 (a) By referring to the VHDL code in **Listing Q3(a)**, write the suitable code for the **`Entity`** part.

(3 marks)

```
architecture gates of two_gates is
Signal    C: bit
begin
 C <= A and B; --concurrent
 E <= C or D;  --statement
End gates;
```

Listing Q3(a)

(b) Convert the Data Flow modeling in **Listing Q3(a)** to the Behavior modeling description.

(5 marks)

Q4 (a) Derive the excitation equations for D1 and D0 in **Figure Q4(a)**.

(2 marks)

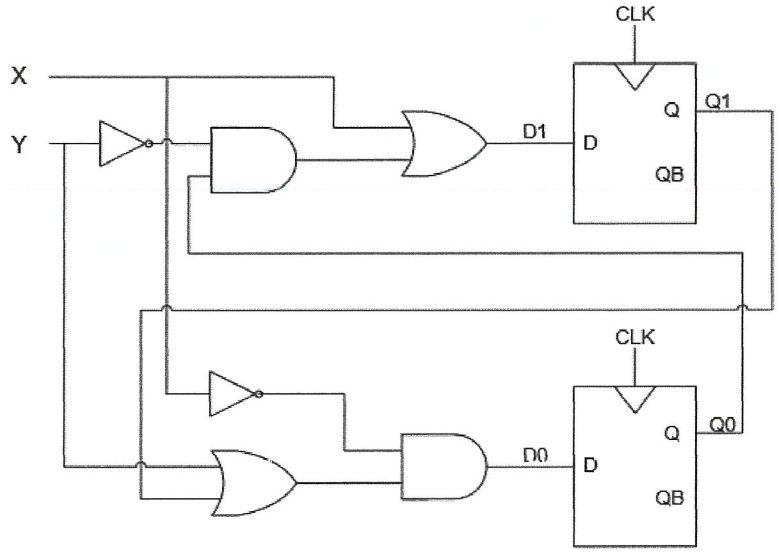

Figure Q4(a): Finite State Machine Analysis

(b) Given the state assignments in **Table Q4(b)**, Create the respective transition table and the state table.

(8 marks)

Table Q4(b): State Assignments:

S	Q1	Q0
A	0	1
B	1	0
U1	0	0
U2	1	1

(c) Based on **Table Q4(b)**, a used state will be reached in one clock cycle under all possible input conditions. For unused states U1 = 00 and U2 = 11, determine the input combinations for which this state machine is unsafe (if any).

(4 marks)

Q5 (a) Write the VHDL code for finite state machine in **Figure Q5(a)**.

(11 marks)

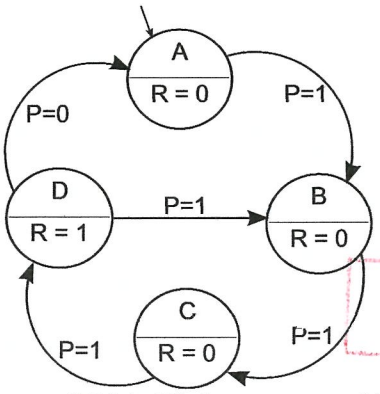

Figure Q5(a): Finite state machine