UTHM
Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2017/2018

COURSE NAME	:	COMPUTER ARCHITECTURE AND ORGANIZATION
COURSE CODE	:	BEC30303
PROGRAMME CODE	:	BEJ
EXAMINATION DATE	:	JUNE/JULY 2018
DURATION	:	3 HOURS
INSTRUCTION	:	ANSWER **ALL** QUESTIONS IN THE QUESTION BOOKLET

THIS QUESTION PAPER CONSISTS OF **ELEVEN (11)** PAGES

SECTION A (OBJECTIVE QUESTIONS)

Q1 The processor keeps track of the results of its operations using a flags called _____

a) Conditional code flags
b) Test output flags
c) Type flags
d) None of the mentioned

(1 mark)

Q2 In a carry-ripple n-bit adder, to find out if an overflow as occurred we make use of _____

a) AND gate
b) NAND gate
c) NOR gate
d) XOR gate

(2 marks)

Q3 When the process is returned after an interrupt service _____ should be loaded again.

i. Condition codes
ii. Register contents
iii. Return addresses
iv. Stack contents

a) i and ii
b) i and iv
c) iii and iv
d) ii, iii, and iv

(2 marks)

Q4 The most important objective of the Universal Serial Bus (USB) is to provide _____

i. Asynchronous data transfer
ii. Easy device connection
iii. Isochronous transmission
iv. Plug and play

a) i, ii, and iii
b) i, ii, and iv
c) i, iii, and iv
d) ii, iii, and iv

(2 marks)

Q5 The instruction, Add LOCA, R0 does _____

a) Adds the value of LOCA to R0 and stores in the temp register
b) Adds the value of R0 to the address of LOCA
c) Adds the values of both LOCA and R0 and stores it in R0
d) Adds the value of LOCA with a value in accumulator and stores it in R0

(2 marks)

Q6 Which register in the processor is single directional?
a) MAR
b) MDR
c) PC
d) Temp

(2 marks)

Q7 The effectiveness of the cache memory is based on the property of _____
a) Memory size
b) Locality of reference
c) Memory localization
d) None of the mentioned

(1 mark)

Q8 A memory organisation that can hold up to 1024 bits and has a minimum of 10 address lines can be organised into _____
a) 128 X 8
b) 256 X 4
c) 512 X 2
d) 1024 X 1

(2 marks)

Q9 The aim of virtual memory organisation are
i. To provide effective memory access
ii. To provide better memory transfer
iii. To improve the execution of the program
a) i and ii
b) i and iii
c) ii and iii
d) i, ii and iii

(2 marks)

Q10 For a given FINITE number of instructions to be executed, which architecture of the processor provides the fastest execution?
a) ISA
b) ANSA
c) Super-scalar
d) All of the mentioned

(1 mark)

Q11 The average number of steps taken to execute the set of instructions can be made to be less than one by _____
a) ISA
b) Pipelining
c) Super-scaling
d) Sequential

(1 mark)

Q12 If a processor clock is rated as 1250 million cycles per second, then its clock period is _____

a) 1.9×10^{-10} sec
b) 1.6×10^{-9} sec
c) 1.25×10^{-10} sec
d) 8×10^{-10} sec

(2 marks)

Q13 Point out the correct statement(s):

a) All SLAs are enforceable as contracts.
b) Platforms are used to create more easy software.
c) Cloud computing relies on a set of protocols needed to manage inter process communications.
d) Cloud computing is a natural extension of many of the design principles, protocols, plumbing, and systems.

(2 marks)

Q14 An application that needed _____ storage alone might not benefit from a cloud deployment at all.

a) online
b) offline
c) virtual
d) None of the mentioned

(2 marks)

Q15 _____ describes a distribution model in which applications are hosted by a service provider and made available to users.

a) Infrastructure-as-a-Service (IaaS)
b) Platform-as-a-Service (PaaS)
c) Software-as-a-Service (SaaS)
d) Cloud service

(1 marks)

SECTION B (SUBJECTIVE QUESTIONS)

Q16 There are two microprocessors with different instruction format. Each microprocessor requires different amount of time to fetch, decode, execute and store each instruction as shown in **Table Q16.**

Table Q16

Microprocessor	Instruction Type	Time per instruction
CPU X	Two-address format RISC	50 ns
CPU Y	One-address format CISC	40 ns

Assume that the prefix expression needed to be executed is:

$$Z = + * AB * CD$$

(a) Produce the Infix expression of the given operation.

(2 marks)

(b) Construct instruction set for expression in **Q16** using the two-address format RISC.

(5 marks)

(c) Construct instruction set for expression in **Q16** using the one address format CISC.

(5 marks)

(d) Evaluate which microprocessor perform the faster execution time.

(3 marks)

Q17 (a) Data transfer for asynchronous bus are based on the use of handshake between master and slave without bus clock. Explain in detail the processes involved by using an appropriate diagram to support your answer.

(8 marks)

(b) I/O device synchronization is crucial in order to synchronize data transfers due to the rate of transfer to/from devices is slower than the speed of the processor. By using appropriate diagram, differentiate three methods of synchronizations that available based on:

(i) program-controlled I/O,

(2.5 marks)

(ii) interrupts-driven

(2.5 marks)

(iii) direct memory access (DMA)

(2 marks)

Q18 (a) Draw the basic instruction cycle in program execution.

(4 marks)

(b) Based on the block diagram shown in **Figure Q18(b)**, write the step by step operations to execute the following instruction (consisting of fetch instruction/data, execute, and write back steps)

Add R10, R20, R30

using register transfer notation. Assume the last element in the assembly language notation is the destination.

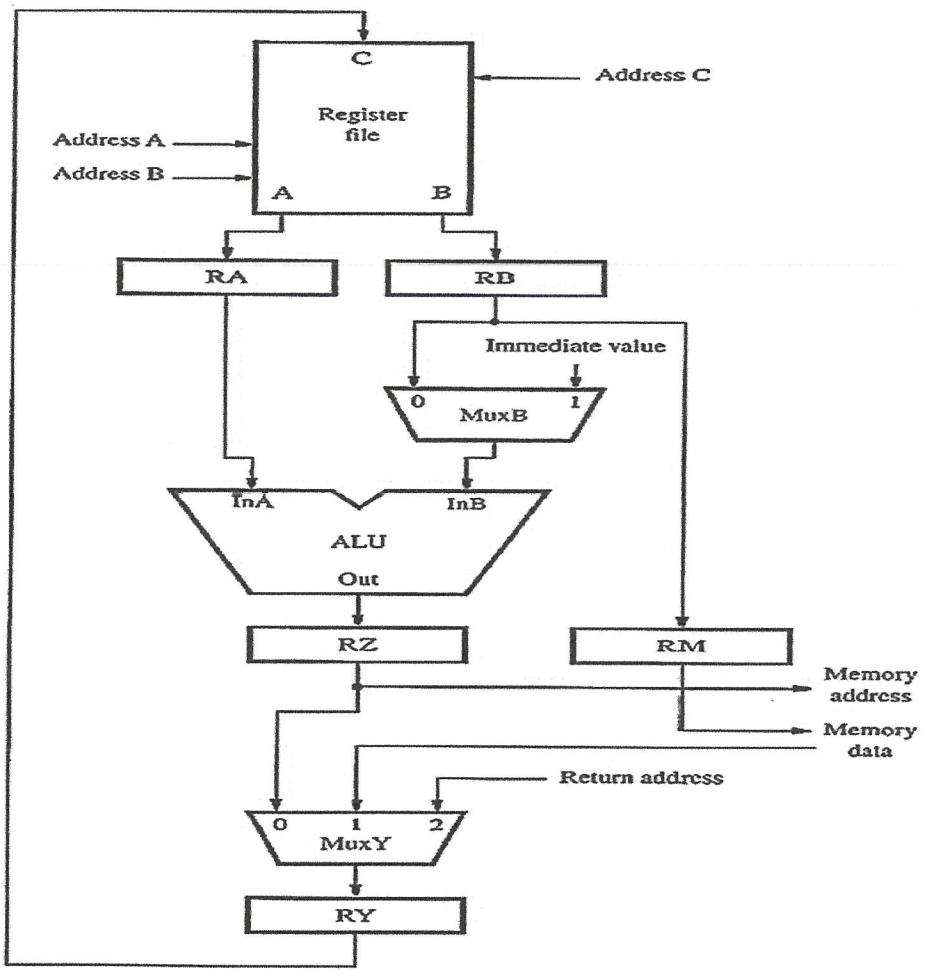

Figure Q18(b)

(11 marks)

Q19 (a) Compare three (3) major differences between Cache Hit and Cache Miss.

	Cache Hit	Cache Miss
1		
2		
3		

(6 marks)

(b) Consider a Direct Mapped Cache with features as in **Table Q19(b),** determine the:

Table Q19(b)

Item	**Value**
Total Number of Cache accessed by CPU	10 access
Total Number of Hit	8 access
Hit Time	4 ns
Miss Penalty	100 ns

(i) Hit rate of the system

(2 marks)

(ii) Miss Rate of the system

(2 marks)

(iii) Average Memory Access Time of the system

(2 marks)

(c) If the cache in **Q19(b)** is replaced with new cache with performance of 97% hit rate and 5 ns hit time, calculate the new Average Memory Access Time for this system.

(3 marks)

Q20 **Figure Q20** shows a space time diagram to execute *n* instructions by CAOTM processor. The instruction cycle comprises 4 steps; fetch (F), decode (D), execute (E), and write back (W). Assume 1 clock cycle = 10 ns.

Time, *ns*	10	20	30	40	50	60	70	80	90	100	110	120	130
Cycle / Instruction	1	2	3	4	5	6	7	8	9	10	11	12	13
1	F	D	E	E	W								
2		F	D		E	E	W						
3			F		D		E	E	W				
4					F		D		E	E	W		
5							F		D		E	E	W

Figure Q20

(a) Identify the value of *n*?

(2 marks)

(b) Classified these instruction cycles' steps into numbers of clock cycle.

(4 marks)

(c) Calculate the total execution time needed by the pipelined computer to execute a C++ program having 3000 instructions.

(4 marks)

(d) Calculate the performance speed up of the pipelined computer over non-pipelined computer to execute similar C++ program in **Q20(c).**

(5 marks)

- END OF QUESTIONS –