Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2017/2018

COURSE NAME	: ADVANCED MICROCONTROLLER
COURSE CODE	: BEC 41103
PROGRAMME	: BEJ
EXAMINATION DATE	: JUNE/JULY 2018
DURATION	: 3 HOURS
INSTRUCTION	: ANSWER **ALL** QUESTIONS

THIS QUESTION PAPER CONSISTS OF **EIGHTEEN (18)** PAGES.

Q1 (a) With visual aid, briefly describe the following achitectures:

(i) Von Neumann architecture.

(5 marks)

(ii) Harvard architecture.

(5 marks)

(b) Describe the drawback of using Harvard architecture for connecting external memories to the CPU.

(3 marks)

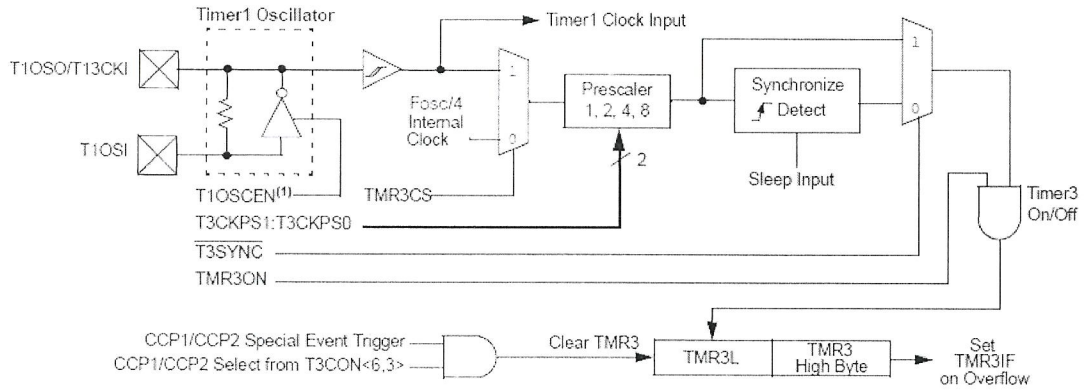
(c) Determine the address of the last location of on-chip program ROM for PIC18 with size of 128KB. Clearly show the steps of solution.

(3 marks)

(d) A PIC18 has 7FFFFH as the address of the last location of its on-chip ROM. Find the size of on-chip ROM for this device in KB. Clearly show the steps of solution.

(4 marks)

Q2 Refering to **Figure Q2**, Timer3 can be utilized as a counter for counting external pulses. Assuming an external clock signal with frequency 1Hz and its pulse is being fed into pin T3CKI (RC0) of the device PIC18F4520.



Note 1: When enable bit, T1OSCEN, is cleared, the inverter and feedback resistor are turned off to eliminate power drain.

Figure Q2

(a) Explain the role of T3CON in Timer3 hardware.

(2 marks)

(b) Determine the value for T3CON, if the Timer3 is programmed as 16-bit mode operation without prescaler.

(4 marks)

(c) Write a complete C program to count pulses of the 1Hz clock signal. Display the TMR3H and TMR3L value on PORTD and PORTB, respectively.

(14 marks)

Q3 (a) Describe TWO (2) differences between asynchronous and synchronous data transmission.

(4 marks)

(b) Consider to transmit character "A" using PIC18 EUSART transmit module, as shown in **Figure Q3(b)** in asynchronous mode. The character shall be framed using 8-bit data with one stop bit and without parity bit. In particular, the device is driven with clock signal of 16MHz and the data is expected to be transmitted in 9600 baud.

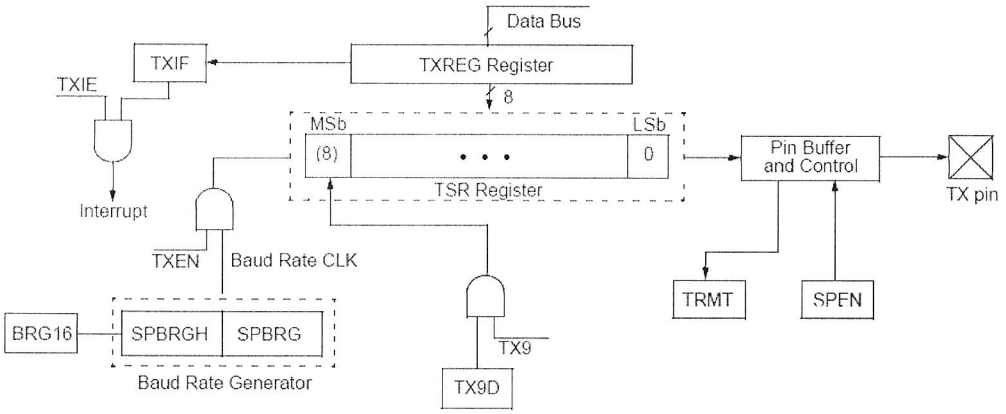


Figure Q3(b)

(i) Calculate the value that will be loaded in the SPBRG register if the BRGH bit is cleared in the TXSTA register.

(4 marks)

(ii) Determine the byte to be loaded in the TXSTA register.

(4 marks)

(iii) Write a C program to transmit the character "A" continuously.

(8 marks)

Q4 (a) Briefly discuss the concept of interrupt in PIC18.

(5 marks)

(b) **Figure Q4(b)** shows INT0-INT2 external hardware interrupts.

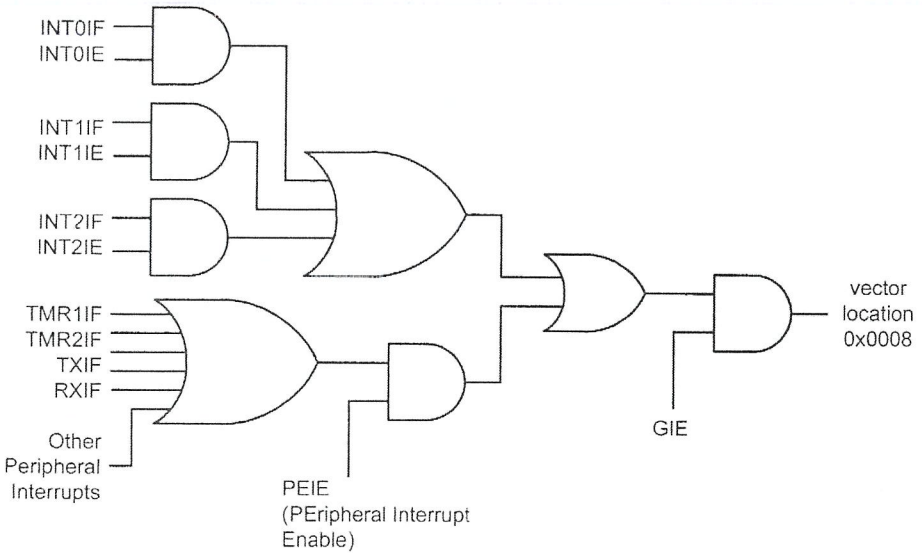


Figure Q4(c)

(i) Determine pin locations for all external hardware interrupts of the PIC18F4520.

(3 marks)

(ii) Write a single instruction to disable all INT0-INT2 interrupts.

(2 marks)

(iii) Write a series of instructions to enable INT2 as high priority external hardware interrupt that activates at negative edge-triggered.

(10 marks)

Q5 (a) Analyze the program in **Figure Q5** and answer the following questions.

(i) Identify the main purpose of the program.

(4 marks)

(ii) Describe the role of TBLPTR in the program.

(2 marks)

(iii) Determine the data to be written to in the program.

(2 marks)

(iv) Examine instructions in Part II of the program **Figure Q5**. Summarize the outcome after executing the instructions in Part II.

(4 marks)

(b) Networking system is needed in many situations to provide connection between different systems or subsystems. Suggest the most suitable network connection between keyboard, mouse PCs and printers without physical cables in the communication and the signal from device can through penetrate walls. Justify the reason of your suggestion.

(4 marks)

(c) WiFi and Bluetooth are two approaches to establish wireless network. Compare between WiFi dan Bluetooth and discuss TWO (2) differences between them.

(4 marks)

```
//Program Figure Q5

#include <p18f4520.h>
void Delay(unsigned int itime);

void main ( ) {
    unsigned char x;
    //Part I
    TBLPTR = (short long) 0x0400;
    TABLAT = 'G';
    _asm TBLWTPOSTINC _endasm
    TABLAT = 'O';
    _asm TBLWTPOSTINC _endasm
    TABLAT = 'O';
    _asm TBLWTPOSTINC _endasm
    TABLAT = 'D';
    _asm TBLWTPOSTINC _endasm
    TABLAT = ' ';
    _asm TBLWTPOSTINC _endasm
    TABLAT = 'B';
    _asm TBLWTPOSTINC _endasm
    TABLAT = 'Y';
    _asm TBLWTPOSTINC _endasm
    TABLAT = 'E';
    _asm TBLWTPOSTINC _endasm
    //Part II
    TBLPTR = (short long)0x0400;
    EECON1bits.EEPGD = 1;
    EECON1bits.CFGS = 0;
    EECON1bits.WREN = 1;
    INTCONbits.GIE = 0;
    EECON2 = 0x55;
    EECON2 = 0xAA;
    EECON1bits.WR=1;
    _asm NOP _endasm
    INTCONbits.GIE = 1;
    EECON1bits.WREN = 0;
    //Part III
    TALPTR = (short long) 0x0400;
    for(x=0;x<8;x++)  {
        _asm TBLRDPOSTINC _endasm
        PORTB = TABLAT;
        Delay(250);  }
}
```

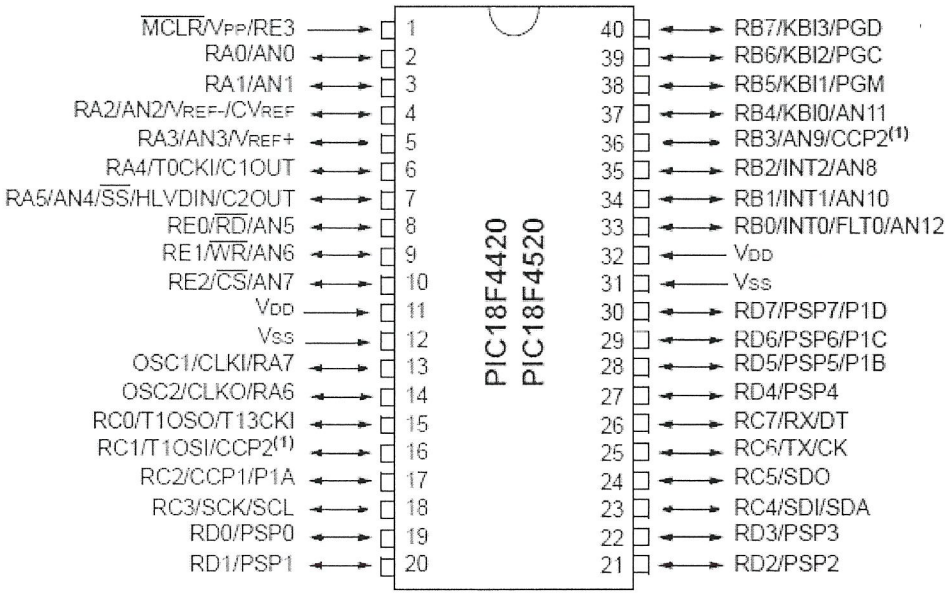
Figure Q5

- END OF QUESTIONS-

FINAL EXAMINATION

SEMESTER / SESSION : SEM II / 2017/2018 PROGRAMME CODE : BEJ
COURSE NAME : ADVANCED MICROCONTROLLER COURSE CODE : BEC 41103

Pin Layout of PIC18F4xxx



FINAL EXAMINATION

SEMESTER / SESSION : SEM II / 2017/2018 PROGRAMME CODE : BEJ
COURSE NAME : ADVANCED MICROCONTROLLER COURSE CODE : BEC 41103

ASCII Table

Dec	Hx	Oct	Char	Dec	Hx	Oct	Html	Chr	Dec	Hx	Oct	Html	Chr	Dec	Hx	Oct	Html	Chr
0	0	000	NUL (null)	32	20	040		Space	64	40	100	@	@	96	60	140	`	`
1	1	001	SOH (start of heading)	33	21	041	!	!	65	41	101	A	A	97	61	141	a	a
2	2	002	STX (start of text)	34	22	042	"	"	66	42	102	B	B	98	62	142	b	b
3	3	003	ETX (end of text)	35	23	043	#	#	67	43	103	C	C	99	63	143	c	c
4	4	004	EOT (end of transmission)	36	24	044	$	$	68	44	104	D	D	100	64	144	d	d
5	5	005	ENQ (enquiry)	37	25	045	%	%	69	45	105	E	E	101	65	145	e	e
6	6	006	ACK (acknowledge)	38	26	046	&	&	70	46	106	F	F	102	66	146	f	f
7	7	007	BEL (bell)	39	27	047	'	'	71	47	107	G	G	103	67	147	g	g
8	8	010	BS (backspace)	40	28	050	(	(	72	48	110	H	H	104	68	150	h	h
9	9	011	TAB (horizontal tab)	41	29	051	)	)	73	49	111	I	I	105	69	151	i	i
10	A	012	LF (NL line feed, new line)	42	2A	052	*	*	74	4A	112	J	J	106	6A	152	j	j
11	B	013	VT (vertical tab)	43	2B	053	+	+	75	4B	113	K	K	107	6B	153	k	k
12	C	014	FF (NP form feed, new page)	44	2C	054	,	,	76	4C	114	L	L	108	6C	154	l	l
13	D	015	CR (carriage return)	45	2D	055	-	-	77	4D	115	M	M	109	6D	155	m	m
14	E	016	SO (shift out)	46	2E	056	.	.	78	4E	116	N	N	110	6E	156	n	n
15	F	017	SI (shift in)	47	2F	057	/	/	79	4F	117	O	O	111	6F	157	o	o
16	10	020	DLE (data link escape)	48	30	060	0	0	80	50	120	P	P	112	70	160	p	p
17	11	021	DC1 (device control 1)	49	31	061	1	1	81	51	121	Q	Q	113	71	161	q	q
18	12	022	DC2 (device control 2)	50	32	062	2	2	82	52	122	R	R	114	72	162	r	r
19	13	023	DC3 (device control 3)	51	33	063	3	3	83	53	123	S	S	115	73	163	s	s
20	14	024	DC4 (device control 4)	52	34	064	4	4	84	54	124	T	T	116	74	164	t	t
21	15	025	NAK (negative acknowledge)	53	35	065	5	5	85	55	125	U	U	117	75	165	u	u
22	16	026	SYN (synchronous idle)	54	36	066	6	6	86	56	126	V	V	118	76	166	v	v
23	17	027	ETB (end of trans. block)	55	37	067	7	7	87	57	127	W	W	119	77	167	w	w
24	18	030	CAN (cancel)	56	38	070	8	8	88	58	130	X	X	120	78	170	x	x
25	19	031	EM (end of medium)	57	39	071	9	9	89	59	131	Y	Y	121	79	171	y	y
26	1A	032	SUB (substitute)	58	3A	072	:	:	90	5A	132	Z	Z	122	7A	172	z	z
27	1B	033	ESC (escape)	59	3B	073	;	;	91	5B	133	[	[	123	7B	173	{	{
28	1C	034	FS (file separator)	60	3C	074	<	<	92	5C	134	\	\	124	7C	174			|
29	1D	035	GS (group separator)	61	3D	075	=	=	93	5D	135	]	]	125	7D	175	}	}
30	1E	036	RS (record separator)	62	3E	076	>	>	94	5E	136	^	^	126	7E	176	~	~
31	1F	037	US (unit separator)	63	3F	077	?	?	95	5F	137	_	_	127	7F	177	&#127;	DEL

Source: www.LookupTables.com

FINAL EXAMINATION

SEMESTER / SESSION : SEM II / 2017/2018 PROGRAMME CODE : BEJ
COURSE NAME : ADVANCED MICROCONTROLLER COURSE CODE : BEC 41103

T3CON: Timer3 Control Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RD16	T3CCP2	T3CKPS1	T3CKPS0	T3CCP1	$\overline{\text{T3SYNC}}$	TMR3CS	TMR3ON
bit 7							bit 0

RD16: 16-bit Read/Write Mode Enable bit
1 = Enables register read/write of Timer3 in one 16-bit operation
0 = Enables register read/write of Timer3 in two 8-bit operations

T3CCP2:T3CCP1: Timer3 and Timer1 to CCPx Enable bits
1x = Timer3 is the capture/compare clock source for the CCP modules
01 = Timer3 is the capture/compare clock source for CCP2;
Timer1 is the capture/compare clock source for CCP1
00 = Timer1 is the capture/compare clock source for the CCP modules

T3CKPS1:T3CKPS0: Timer3 Input Clock Prescale Select bits
11 = 1:8 Prescale value
10 = 1:4 Prescale value
01 = 1:2 Prescale value
00 = 1:1 Prescale value

$\overline{\text{T3SYNC}}$: Timer3 External Clock Input Synchronization Control bit
(Not usable if the device clock comes from Timer1/Timer3.)
When TMR3CS = 1:
1 = Do not synchronize external clock input
0 = Synchronize external clock input
When TMR3CS = 0:
This bit is ignored. Timer3 uses the internal clock when TMR3CS = 0.

TMR3CS: Timer3 Clock Source Select bit
1 = External clock input from Timer1 oscillator or T13CKI (on the rising edge after the first falling edge)
0 = Internal clock (FOSC/4)

TMR3ON: Timer3 On bit
1 = Enables Timer3
0 = Stops Timer3

FINAL EXAMINATION

SEMESTER / SESSION : SEM II / 2017/2018 PROGRAMME CODE : BEJ
COURSE NAME : ADVANCED MICROCONTROLLER COURSE CODE : BEC 41103

TXSTA (Transmit Status and Control Register)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-1	R/W-0
CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D
bit 7							bit 0

CSRC: Clock Source Select bit

Asynchronous mode:
Don't care.

Synchronous mode:
1 = Master mode (clock generated internally from BRG)
0 = Slave mode (clock from external source)

TX9: 9-bit Transmit Enable bit

1 = Selects 9-bit transmission
0 = Selects 8-bit transmission

TXEN: Transmit Enable bit

1 = Transmit enabled
0 = Transmit disabled

Note: SREN/CREN overrides TXEN in Sync mode.

SYNC: EUSART Mode Select bit

1 = Synchronous mode
0 = Asynchronous mode

SENDB: Send Break Character bit

Asynchronous mode:
1 = Send Sync Break on next transmission (cleared by hardware upon completion)
0 = Sync Break transmission completed

Synchronous mode:
Don't care.

BRGH: High Baud Rate Select bit

Asynchronous mode:
1 = High speed
0 = Low speed

Synchronous mode:
Unused in this mode.

TRMT: Transmit Shift Register Status bit

1 = TSR empty
0 = TSR full

TX9D: 9th bit of Transmit Data

Can be address/data bit or a parity bit.

FINAL EXAMINATION

SEMESTER / SESSION : SEM II / 2017/2018 PROGRAMME CODE : BEJ
COURSE NAME : ADVANCED MICROCONTROLLER COURSE CODE : BEC 41103

RCSTA (Receive Status and Control Register)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-x
SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D
bit 7							bit 0

SPEN: Serial Port Enable bit

1 = Serial port enabled (configures RX/DT and TX/CK pins as serial port pins)
0 = Serial port disabled (held in Reset)

RX9: 9-bit Receive Enable bit

1 = Selects 9-bit reception
0 = Selects 8-bit reception

SREN: Single Receive Enable bit

Asynchronous mode:
Don't care.

Synchronous mode – Master:
1 = Enables single receive
0 = Disables single receive
This bit is cleared after reception is complete.

Synchronous mode – Slave:
Don't care.

CREN: Continuous Receive Enable bit

Asynchronous mode:
1 = Enables receiver
0 = Disables receiver

Synchronous mode:
1 = Enables continuous receive until enable bit CREN is cleared (CREN overrides SREN)
0 = Disables continuous receive

ADDEN: Address Detect Enable bit

Asynchronous mode 9-bit (RX9 = 1):
1 = Enables address detection, enables interrupt and loads the receive buffer when RSR<8> is set
0 = Disables address detection, all bytes are received and ninth bit can be used as parity bit

Asynchronous mode 9-bit (RX9 = 0):
Don't care.

FERR: Framing Error bit

1 = Framing error (can be updated by reading RCREG register and receiving next valid byte)
0 = No framing error

OERR: Overrun Error bit

1 = Overrun error (can be cleared by clearing bit CREN)
0 = No overrun error

RX9D: 9th bit of Received Data

This can be address/data bit or a parity bit and must be calculated by user firmware.

FINAL EXAMINATION

SEMESTER / SESSION : SEM II / 2017/2018 PROGRAMME CODE : BEJ
COURSE NAME : ADVANCED MICROCONTROLLER COURSE CODE : BEC 41103

PIR1 (Peripheral Interrupt Request (Flag) Register 1

R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
PSPIF(1)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF
bit 7							bit 0

PSPIF: Parallel Slave Port Read/Write Interrupt Flag bit(1)
1 = A read or a write operation has taken place (must be cleared in software)
0 = No read or write has occurred

Note 1: This bit is unimplemented on 28-pin devices and will read as '0'.

ADIF: A/D Converter Interrupt Flag bit
1 = An A/D conversion completed (must be cleared in software)
0 = The A/D conversion is not complete

RCIF: EUSART Receive Interrupt Flag bit
1 = The EUSART receive buffer, RCREG, is full (cleared when RCREG is read)
0 = The EUSART receive buffer is empty

TXIF: EUSART Transmit Interrupt Flag bit
1 = The EUSART transmit buffer, TXREG, is empty (cleared when TXREG is written)
0 = The EUSART transmit buffer is full

SSPIF: Master Synchronous Serial Port Interrupt Flag bit
1 = The transmission/reception is complete (must be cleared in software)
0 = Waiting to transmit/receive

CCP1IF: CCP1 Interrupt Flag bit
Capture mode:
1 = A TMR1 register capture occurred (must be cleared in software)
0 = No TMR1 register capture occurred
Compare mode:
1 = A TMR1 register compare match occurred (must be cleared in software)
0 = No TMR1 register compare match occurred
PWM mode:
Unused in this mode.

TMR2IF: TMR2 to PR2 Match Interrupt Flag bit
1 = TMR2 to PR2 match occurred (must be cleared in software)
0 = No TMR2 to PR2 match occurred

TMR1IF: TMR1 Overflow Interrupt Flag bit
1 = TMR1 register overflowed (must be cleared in software)
0 = TMR1 register did not overflow

FINAL EXAMINATION

SEMESTER / SESSION : SEM II / 2017/2018 PROGRAMME CODE : BEJ
COURSE NAME : ADVANCED MICROCONTROLLER COURSE CODE : BEC 41103

PIR2 (Peripheral Interrupt Request (Flag) Register 2

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OSCFIF	CMIF	—	EEIF	BCLIF	HLVDIF	TMR3IF	CCP2IF
bit 7							bit 0

OSCFIF: Oscillator Fail Interrupt Flag bit

1 = Device oscillator failed, clock input has changed to INTOSC (must be cleared in software)
0 = Device clock operating

CMIF: Comparator Interrupt Flag bit

1 = Comparator input has changed (must be cleared in software)
0 = Comparator input has not changed

Unimplemented: Read as '0'

EEIF: Data EEPROM/Flash Write Operation Interrupt Flag bit

1 = The write operation is complete (must be cleared in software)
0 = The write operation is not complete or has not been started

BCLIF: Bus Collision Interrupt Flag bit

1 = A bus collision occurred (must be cleared in software)
0 = No bus collision occurred

HLVDIF: High/Low-Voltage Detect Interrupt Flag bit

1 = A high/low-voltage condition occurred (direction determined by VDIRMAG bit, HLVDCON<7>)
0 = A high/low-voltage condition has not occurred

TMR3IF: TMR3 Overflow Interrupt Flag bit

1 = TMR3 register overflowed (must be cleared in software)
0 = TMR3 register did not overflow

CCP2IF: CCPx Interrupt Flag bit

Capture mode:

1 = A TMR1 register capture occurred (must be cleared in software)
0 = No TMR1 register capture occurred

Compare mode:

1 = A TMR1 register compare match occurred (must be cleared in software)
0 = No TMR1 register compare match occurred

PWM mode:

Unused in this mode.

FINAL EXAMINATION

SEMESTER / SESSION : SEM II / 2017/2018 PROGRAMME CODE : BEJ
COURSE NAME : ADVANCED MICROCONTROLLER COURSE CODE : BEC 41103

EECON1 (EEPROM Control Register)

R/W-x	R/W-x	U-0	R/W-0	R/W-x	R/W-0	R/S-0	R/S-0
EEPGD	CFGS	—	FREE	WRERR	WREN	WR	RD
bit 7							bit 0

EEPGD: Flash Program or Data EEPROM Memory Select bit

1 = Access Flash program memory
0 = Access data EEPROM memory

CFGS: Flash Program/Data EEPROM or Configuration Select bit

1 = Access Configuration registers
0 = Access Flash program or data EEPROM memory

Unimplemented: Read as '0'

FREE: Flash Row Erase Enable bit

1 = Erase the program memory row addressed by TBLPTR on the next WR command (cleared by completion of erase operation)
0 = Perform write only

WRERR: Flash Program/Data EEPROM Error Flag bit

1 = A write operation is prematurely terminated (any Reset during self-timed programming in normal operation, or an improper write attempt)
0 = The write operation completed

Note: When a WRERR occurs, the EEPGD and CFGS bits are not cleared. This allows tracing of the error condition.

WREN: Flash Program/Data EEPROM Write Enable bit

1 = Allows write cycles to Flash program/data EEPROM
0 = Inhibits write cycles to Flash program/data EEPROM

WR: Write Control bit

1 = Initiates a data EEPROM erase/write cycle or a program memory erase cycle or write cycle. (The operation is self-timed and the bit is cleared by hardware once write is complete. The WR bit can only be set (not cleared) in software.)
0 = Write cycle to the EEPROM is complete

RD: Read Control bit

1 = Initiates an EEPROM read (Read takes one cycle. RD is cleared in hardware. The RD bit can only be set (not cleared) in software. RD bit cannot be set when EEPGD = 1 or CFGS = 1.)
0 = Does not initiate an EEPROM read

FINAL EXAMINATION

SEMESTER / SESSION : SEM II / 2017/2018 PROGRAMME CODE : BEJ
COURSE NAME : ADVANCED MICROCONTROLLER COURSE CODE : BEC 41103

INTCON Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF
bit 7							bit 0

GIE/GIEH. Global Interrupt Enable bit

When IPEN = 0:
1 = Enables all unmasked interrupts
0 = Disables all interrupts

When IPEN = 1:
1 = Enables all high priority interrupts
0 = Disables all interrupts

PEIE/GIEL: Peripheral Interrupt Enable bit

When IPEN = 0:
1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts

When IPEN = 1:
1 = Enables all low priority peripheral interrupts
0 = Disables all low priority peripheral interrupts

TMR0IE: TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 overflow interrupt
0 = Disables the TMR0 overflow interrupt

INT0IE: INT0 External Interrupt Enable bit
1 = Enables the INT0 external interrupt
0 = Disables the INT0 external interrupt

RBIE: RB Port Change Interrupt Enable bit
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

TMR0IF: TMR0 Overflow Interrupt Flag bit
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

INT0IF: INT0 External Interrupt Flag bit
1 = The INT0 external interrupt occurred (must be cleared in software)
0 = The INT0 external interrupt did not occur

RBIF: RB Port Change Interrupt Flag bit
1 = At least one of the RB7:RB4 pins changed state (must be cleared in software)
0 = None of the RB7:RB4 pins have changed state

Note: A mismatch condition will continue to set this bit. Reading PORTB will end the mismatch condition and allow the bit to be cleared.

FINAL EXAMINATION

SEMESTER / SESSION : SEM II / 2017/2018 PROGRAMME CODE : BEJ
COURSE NAME : ADVANCED MICROCONTROLLER COURSE CODE : BEC 41103

INTCON2 Register

R/W-1	R/W-1	R/W-1	R/W-1	U-0	R/W-1	U-0	R/W-1
$\overline{\text{RBPU}}$	INTEDG0	INTEDG1	INTEDG2	—	TMR0IP	—	RBIP
bit 7							bit 0

$\overline{\text{RBPU}}$: PORTB Pull-up Enable bit
1 = All PORTB pull-ups are disabled
0 = PORTB pull-ups are enabled by individual port latch values

INTEDG0: External Interrupt 0 Edge Select bit
1 = Interrupt on rising edge
0 = Interrupt on falling edge

INTEDG1: External Interrupt 1 Edge Select bit
1 = Interrupt on rising edge
0 = Interrupt on falling edge

INTEDG2: External Interrupt 2 Edge Select bit
1 = Interrupt on rising edge
0 = Interrupt on falling edge

Unimplemented: Read as '0'

TMR0IP: TMR0 Overflow Interrupt Priority bit
1 = High priority
0 = Low priority

Unimplemented: Read as '0'

RBIP: RB Port Change Interrupt Priority bit
1 = High priority
0 = Low priority

FINAL EXAMINATION

SEMESTER / SESSION : SEM II / 2017/2018 PROGRAMME CODE : BEJ
COURSE NAME : ADVANCED MICROCONTROLLER COURSE CODE : BEC 41103

INTCON3 Register

R/W-1	R/W-1	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
INT2IP	INT1IP	—	INT2IE	INT1IE	—	INT2IF	INT1IF
bit 7							bit 0

INT2IP: INT2 External Interrupt Priority bit
1 = High priority
0 = Low priority

INT1IP: INT1 External Interrupt Priority bit
1 = High priority
0 = Low priority

Unimplemented: Read as '0'

INT2IE: INT2 External Interrupt Enable bit
1 = Enables the INT2 external interrupt
0 = Disables the INT2 external interrupt

INT1IE: INT1 External Interrupt Enable bit
1 = Enables the INT1 external interrupt
0 = Disables the INT1 external interrupt

Unimplemented: Read as '0'

INT2IF: INT2 External Interrupt Flag bit
1 = The INT2 external interrupt occurred (must be cleared in software)
0 = The INT2 external interrupt did not occur

INT1IF: INT1 External Interrupt Flag bit
1 = The INT1 external interrupt occurred (must be cleared in software)
0 = The INT1 external interrupt did not occur

FINAL EXAMINATION

SEMESTER / SESSION : SEM II / 2017/2018 PROGRAMME CODE : BEJ
COURSE NAME : ADVANCED MICROCONTROLLER COURSE CODE : BEC 41103

RCON Register

R/W-0	R/W-1(1)	U-0	R/W-1	R-1	R-1	R/W-0(1)	R/W-0
IPEN	SBOREN	—	$\overline{RI}$	$\overline{TO}$	$\overline{PD}$	$\overline{POR}$	$\overline{BOR}$
bit 7							bit 0

IPEN: Interrupt Priority Enable bit
1 = Enable priority levels on interrupts
0 = Disable priority levels on interrupts (PIC16XXX Compatibility mode)

SBOREN: Software BOR Enable bit(1)
For details of bit operation, see Register 4-1.

Note 1. Actual Reset values are determined by device configuration and the nature of the device Reset. See Register 4-1 for additional information.

Unimplemented: Read as '0'

$\overline{RI}$: RESET Instruction Flag bit
For details of bit operation, see Register 4-1.

$\overline{TO}$: Watchdog Time-out Flag bit
For details of bit operation, see Register 4-1.

$\overline{PD}$: Power-down Detection Flag bit
For details of bit operation, see Register 4-1.

$\overline{POR}$: Power-on Reset Status bit
For details of bit operation, see Register 4-1.

$\overline{BOR}$: Brown-out Reset Status bit
For details of bit operation, see Register 4-1.