Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2017/2018

COURSE NAME	:	VLSI SYSTEM DESIGN
COURSE CODE	:	BEC 42003
PROGRAMME	:	BEJ
EXAMINATION DATE	:	DECEMBER 2017 / JANUARY 2018
DURATION	:	3 HOURS
INSTRUCTION	:	ANSWER ALL QUESTIONS

THIS QUESTION PAPER CONSISTS OF **EIGHT (8)** PAGES

Q1 (a) Metal Oxide Semiconductor (MOS) has driven the advancement of the modern computer. However, nMOS and pMOS transistors are not a perfect switch. With the aid of a diagram, explain why the pMOS transistor poorly passes logic '0', but good in passing logic '1'.

(5 marks)

(b) Figure Q1(b) shows an input-output block diagram (IOBD) of a half-adder.

(i) Derive Boolean equation of the output signals for the given adder.

(3 marks)

(ii) Sketch the CMOS transistor-level circuit for the "Sum" function using a minimum number of transistors.

(5 marks)

(iii) Sketch logic graph and stick diagram for a minimum layout area.

(6 marks)

(iv) Estimate the area of the layout from the stick diagram. Given the aspect ratio of the pMOS and nMOS transistors are $(W/L)_p = (18\lambda/2\lambda)$ and $(W/L)_n = (6\lambda/2\lambda)$ respectively. Please ignore body contact for both transistors.

(6 marks)

Q2 (a) An nMOS transistor has a 35 Å gate oxide. Given the electron mobility $\mu_n = 600$ $cm^2/v{\cdot}s$ and the gate dimensions are $W = 0.06$ µm and $L = 0.12$ µm.

(i) Determine the gate capacitance, C_G, in fF. Assume that $\varepsilon_{ins} = 3.9\varepsilon_o$ with $\varepsilon_o = 8.854 \times 10^{-14}$ F/cm.

(5marks)

(ii) Calculate the device transconductance, β_n, in unit of $\mu A/V^2$.

(4 marks)

(iii) Given the threshold V_{Tn} voltage is 0.4 V and power supply is 1.2 V, use the square law models to find the drain current if $V_{GS} = 1$ V, $V_{DS} = 0.8$ V and $V_{SB} = 0$ V. Assume that channel length modulation, $\lambda = 0.6$.

(6 marks)

(b) Figure Q2(b) shows the implementation of the CMOS inverter as a buffer in a VLSI interconnect.

(i) Estimate signal delay at node x. The parameters of the inverter and interconnect wire are given in Table Q2(b).

(ii) Discuss options to minimize signal delay at node x.

Q3 (a) Figure Q3(a)(i) and (a)(ii) show the layout of two CMOS inverters. Explain why the layout in Figure Q3(a)(i) is preferable as compare to the layout in Figure Q3(a)(ii) if the hole and electron mobility for the pMOS and nMOS transistors are 200 $cm^2/v{\cdot}s$ and 600 $cm^2/v{\cdot}s$ respectively.

(7 marks)

(b) Figure Q3(b)(i) and (b)(ii) show how the contacts are used in the layout design. Which layout is consider to be better in term of performance? Justify your answer.

(8 marks)

(c) For the circuit in Figure Q3(c)(i)

(i) Name the circuit and state the function of the feedback loop.

(2 marks)

(ii) Sketch the signal waveform at node *F* for the inputs given in Figure Q2(c)(ii).

(3 marks)

(d) Estimate the hold time (retention time) of a DRAM if the minimum voltage that can be recognized as logic one is 0.7 V and the initial voltage on the capacitor is 1 V. Given $V_{DD} = 1$ V.

(5 marks)

Q4 For the equation $c = 2a + b$, apply RTL design methodology to:

(a) Obtain the functional block diagram (FBD) of the datapath unit for the computation block by using one adder and two registers.

(7 marks)

(b) Derive the ASM chart and control sequence table for the control unit.

(8 marks)

(c) Derive the Boolean equations for the next-state and control vector signals for the control unit.

(6 marks)

(d) Estimate the maximum operating frequency of the design if the critical path delay (cpd) of the adder and register are 150 ns and 10 ns respectively.

(4 marks)

- END OF QUESTIONS –

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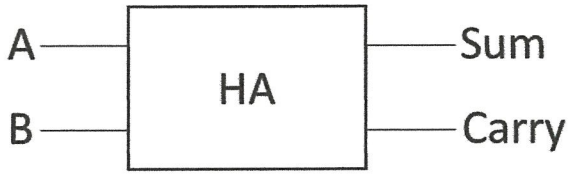

Figure Q1(b)

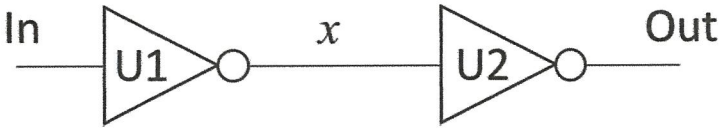

Figure Q2(b)

Table Q2(b)

Parameter	Value	Unit
Power supply, V_{DD}	1.2	V
Gate capacitance U1	0.7	fF
Output capacitance U1	0.5	fF
Gate capacitance U2	1.0	fF
Output capacitance U2	0.8	fF
Intrinsic resistance U1	1000	Ω
Intrinsic resistance U2	1200	Ω
Wire capacitance	2.6	fF
Wire resistance	5.0	Ω
P device transconductance, β_p	1381.2	μA / V^2
N device transconductance, β_n	1266.1	μA / V^2

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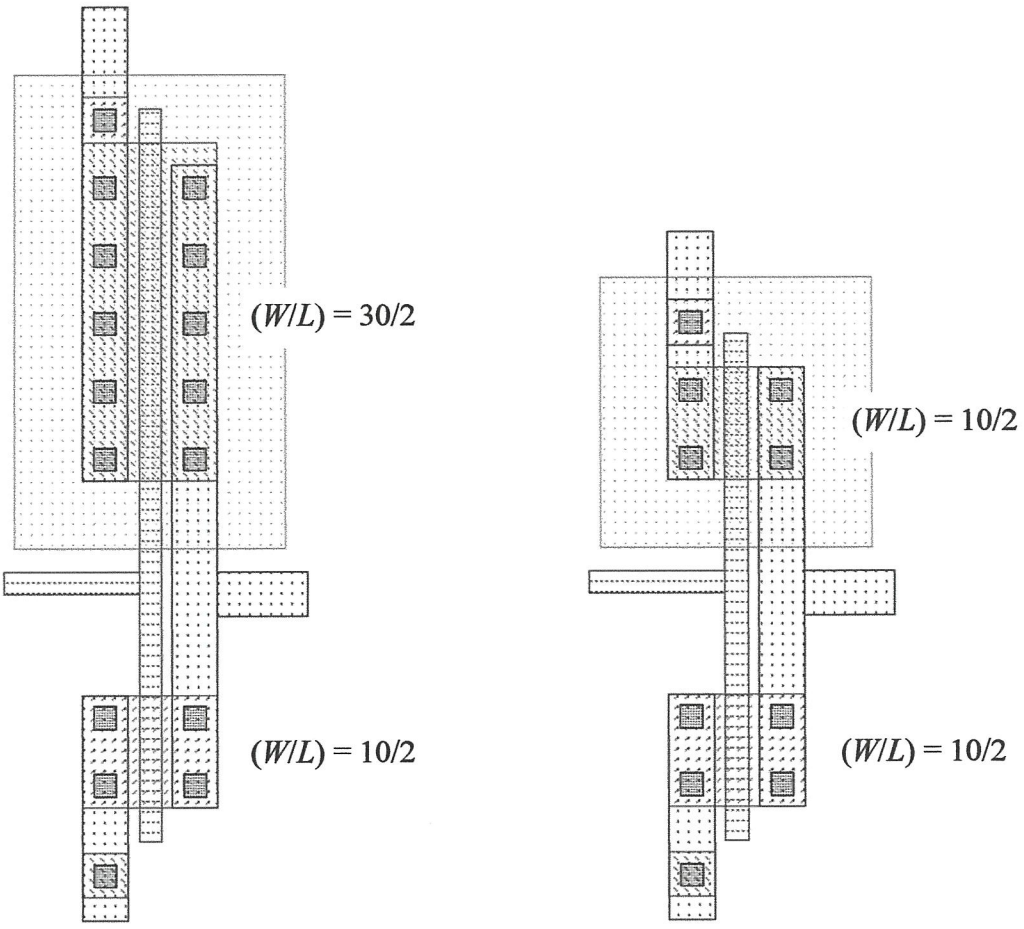

(i) (ii)

Figure Q3(a)

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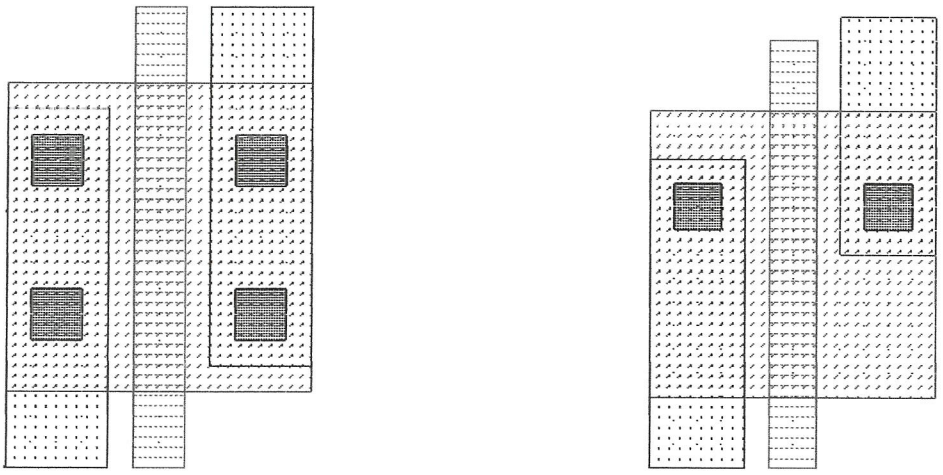
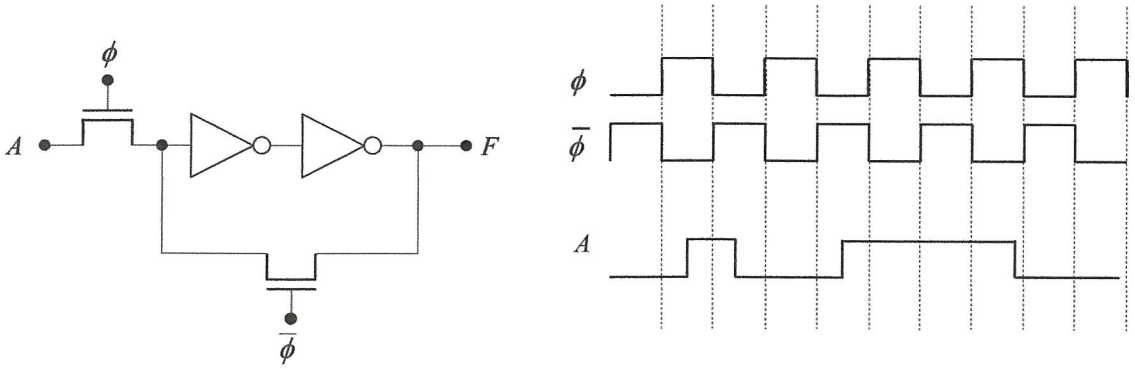


(i) (ii)

Figure Q3(b)



(i) (ii)

Figure Q3(c)

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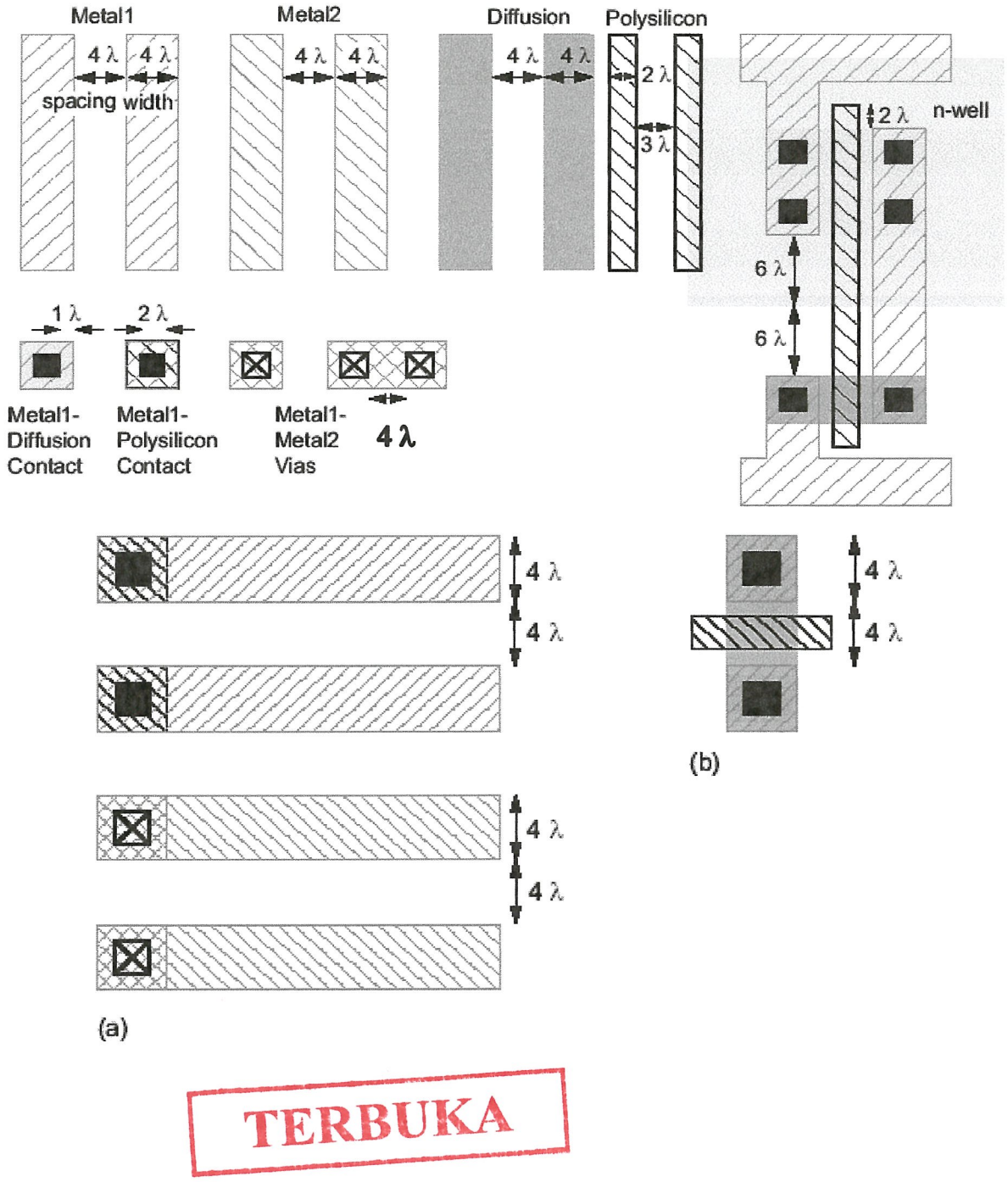
Layout design rules



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EQUATIONS

Device transconductance

$$\beta_n = (\mu_n C_{ox})\left(\frac{W}{L}\right)_n, \quad \beta_p = (\mu_p C_{ox})\left(\frac{W}{L}\right)_p$$

The square law model

MOSFET's drain current for linear region

$$I_{Dn} = \frac{\beta_n}{2}\left[2(V_{GS} - V_{Tn})V_{DS} - V_{DS}^2\right]$$

$$I_{Dp} = \frac{\beta_p}{2}\left[2(V_{SG} - |V_{Tp}|)V_{SD} - V_{SD}^2\right]$$

MOSFET's drain current at $V_{DS} = V_{sat}$

$$V_{sat} = V_{GS} - V_t$$

$$I_{Dn,sat} = \frac{\beta_n}{2}(V_{GS} - V_{Tn})^2$$

$$I_{Dp,sat} = \frac{\beta_p}{2}(V_{SG} - |V_{Tp}|)^2$$

MOSFET's drain current at saturation region

$$I_{Dn} = \frac{\beta_n}{2}(V_{GS} - V_{Tn})^2[1 + \lambda(V_{DS} - V_{sat})]$$

$$I_{Dp} = \frac{\beta_p}{2}(V_{SG} - |V_{Tp}|)^2[1 + \lambda(V_{SD} - V_{sat})]$$