Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2017/2018

COURSE NAME	:	VLSI DESIGN
COURSE CODE	:	BED 30303
PROGRAMME	:	BEJ
EXAMINATION DATE	:	DECEMBER 2017/JANUARY 2018
DURATION	:	3 HOURS
INSTRUCTION	:	ANSWER **ALL** QUESTIONS

THIS QUESTION PAPER CONSISTS OF **SIX (6)** PAGES

Q1 (a) (i) State **TWO (2)** advantages of integrated circuit (IC)

(4 marks)

(ii) Explain clearly the term 'More Than Moore'.

(4 marks)

(b) **Figure Q1(b)** shows a stick diagram of logical circuit using fully complementary static CMOS.

(i) Analyse the circuit and draw the electrically equivalent transistor level schematic circuit of the stick diagram.

(10 marks)

(ii) Determine the logic equation for the output Y.

(2 marks)

Q2 (a) Discuss **TWO (2)** advantages and **TWO (2)** disadvantages of designing a logic circuit at transistor level using pseudo-nMOS method.

(4 marks)

(b) Elaborate with appropriate diagram the violation of monotonicity requirement in the dynamic logic circuits.

(5 marks)

(c) Design a dynamic logic circuit with minimum number of transistors to realize the logic function of $F = \overline{MN + (W + Z)(X + YV)}$. The circuit must be able to eliminate a contention problem.

(11 marks)

Q3 (a) List **TWO (2)** sources of leakage current in CMOS transistor and explain clearly the reason why leakage current increases with the advancement of technology scaling in CMOS transistor.

(4 marks)

(b) A logic function is given by equation $Y = \overline{(A+BC)(D+E)}$

(i) Design a transistor level circuit utilising fully complementary static CMOS logic method to implement the function using minimum number of transistor. The circuit need to have a minimum parasitic delay.

(6 marks)

(ii) Determine the size of each transistor to be used in the design such that the circuit will have an equivalent driving capability of an inverter. Also calculate the minimum parasitic delay. Assume that the minimum length for the transistor is 2λ and the mobility ratio of electron and holes is 3.

(10 marks)

Q4 (a) A negative-level sensitive (negative triggered) D latch circuit can be designed using a multiplexer and two inverters as shown in **Figure Q4(a)**.

(i) Draw the circuit at transistor level and obtain the equation for the output of the circuit, Q. The multiplexer must be design using transmission gate.

(8 marks)

(ii) Analyse the circuit and determine when the circuit is in 'transparent' form and 'opaque' form with regards to the clock input. Assess the output at these two forms.

(6 marks)

(b) Create a positive or leading edge triggered D flip-flop using minimum number of transistors. Draw and label completely the circuit.

(6 marks)

Q5 (a) **Figure Q5(a)** is a block diagram of 2-to-4 decoder with enable input (E).

(i) Construct a truth table for the encoder and obtain the equation for each output.

(10 marks)

(ii) Design at transistor level the circuit for the output D_2 of the decoder using pseudo-nMOS logic with minimum number of transistors.

(4 marks)

(b) Draw at transistor level a 6T SRAM circuit. Show clearly the word and bit lines for the circuit.

(6 marks)

– END OF QUESTIONS –

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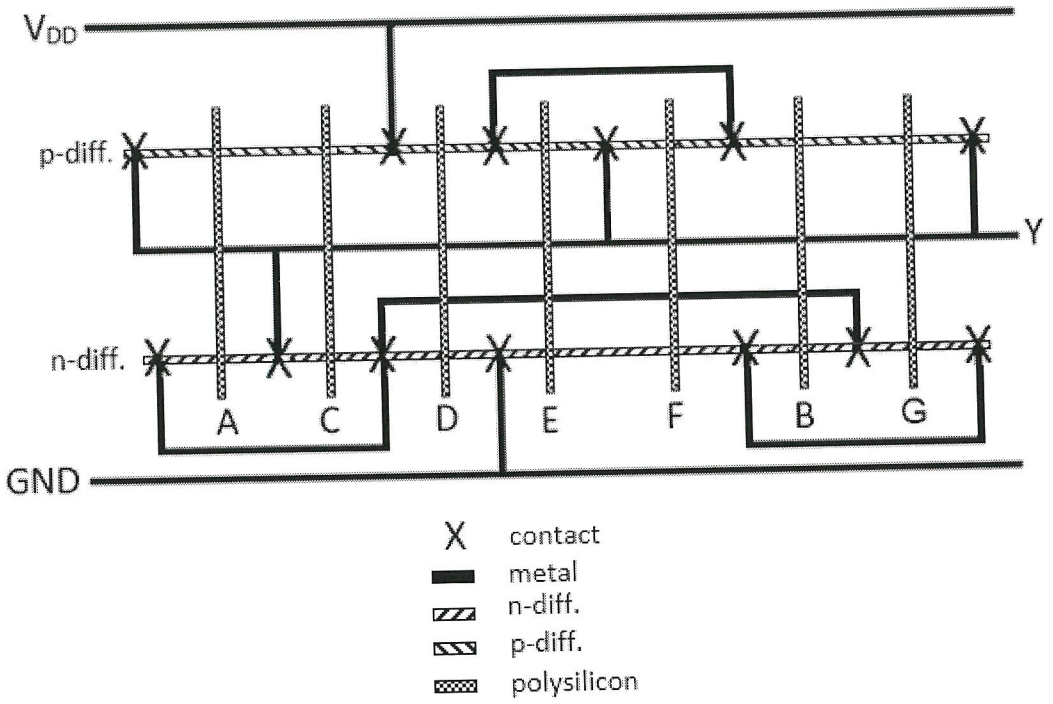

Figure Q1(b)

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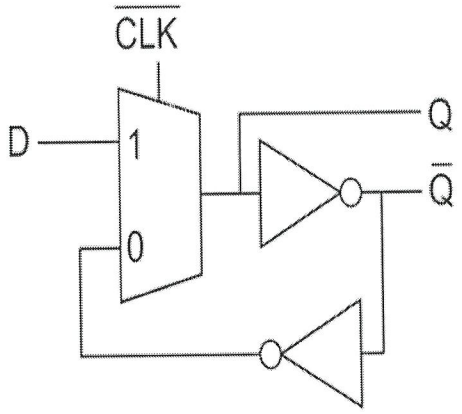

Figure Q4(a)

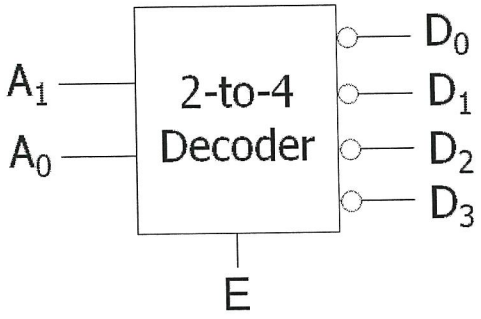

Figure Q5(a)