UTHM
Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2017/2018

COURSE NAME	:	VLSI DESIGN
COURSE CODE	:	BED 30303
PROGRAMME CODE	:	BEJ
EXAMINATION DATE	:	JUNE/JULY 2018
DURATION	:	3 HOURS
INSTRUCTION	:	ANSWER **ALL** QUESTIONS

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THIS QUESTION PAPER CONSISTS OF **FIVE (5)** PAGES

(b) Determine the size for all transistors of the circuit illustrated in **Figure Q3(b)** such that the circuit will have an equivalent driving capability on an inverter. Given the minimum transistor length (L) is 2λ and the width (W) is 3λ and the mobility of the electron is 3 times of the hole's mobility.

(13 marks)

Q4 (a) A two non-overlapping clock can be generated by using NOR-based structure like unclocked SR latch circuit.

(i) Illustrate the circuit of the two non-overlapping clock at gate level.

(4 marks)

(ii) Draw the circuit at transistor level using a full complementary static CMOS with a minimum number of transistors.

(6 marks)

(b) An edge triggered D flip-flop circuit shown in **Figure Q4(b)** is designed using two non-overlapping clock ϕ_1 and ϕ_2.

(i) Sketch the timing diagram of these two clocks for two cycles and explain why the clocks have to be non-overlapped.

(4 marks)

(ii) Analyse the circuit to describe the operation of the D flip-flop according to the clock.

(6 marks)

Q5 A block diagram of 4-to-1 multiplexer (MUX) is shown in **Figure Q5**. Design the 4-to-1 multiplexer using 2-to-1 multiplexer. The 2-to-1 multiplexer must be designed using a tristate method.

(10 marks)

– END OF QUESTIONS –

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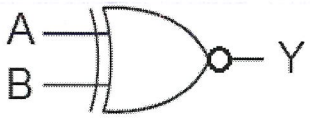

Figure Q2(b)

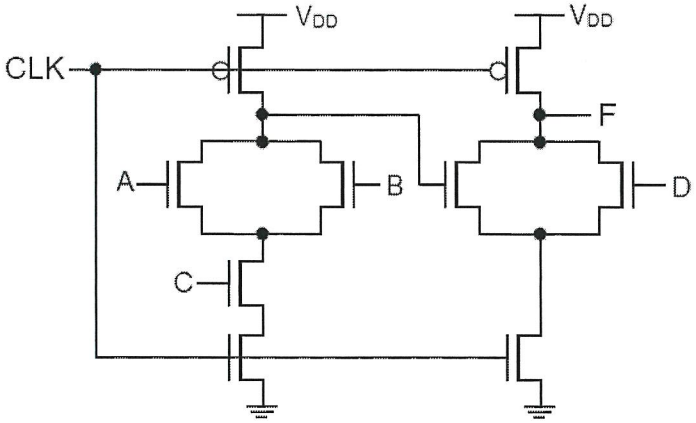

Figure Q2(c)

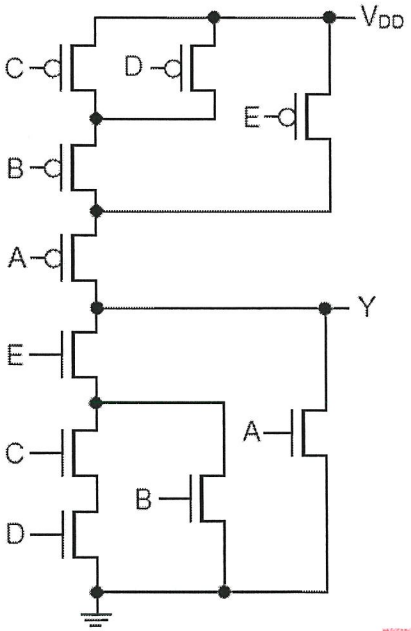

Figure Q3(b)

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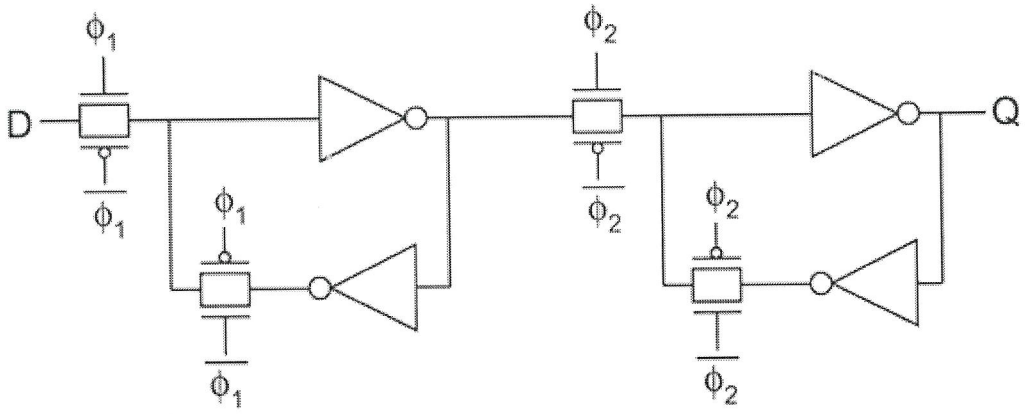

Figure Q4(b)

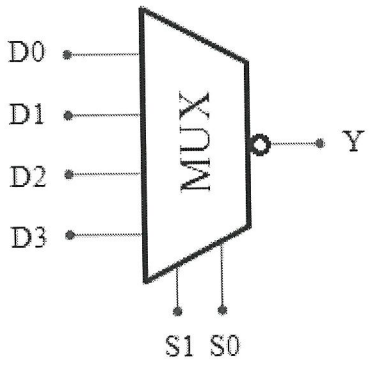

Figure Q5

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