Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER 1
SESSION 2017/2018

COURSE NAME	:	ANALOG ELECTRONICS
COURSE CODE	:	BEL10203
PROGRAMME	:	BEJ/BEV
EXAMINATION DATE	:	DISEMBER 2017/JANUARY 2018
DURATION	:	3 HOURS
INSTRUCTION	:	ANSWER **ALL** QUESTIONS

THIS QUESTION PAPER CONSISTS OF **EIGHT (8)** PAGES

Q1 (a) Materials can be classified in terms of their electrical properties. With the aid of diagram:

(i) Distinguish the energy diagrams of a conductor, an insulator, and a semiconductor.

(6 marks)

(ii) Explain how an N-type semiconductor is formed.

(2 marks)

(b) Diodes are used in various circuit applications such as in voltage regulator, clipper and clamper circuit. Design a diode clamper to generate the output voltage, *Vo* from the input voltage, *Vi* as shown in **Figure Q1(b).** Assume ideal diode model in your design.

(8 marks)

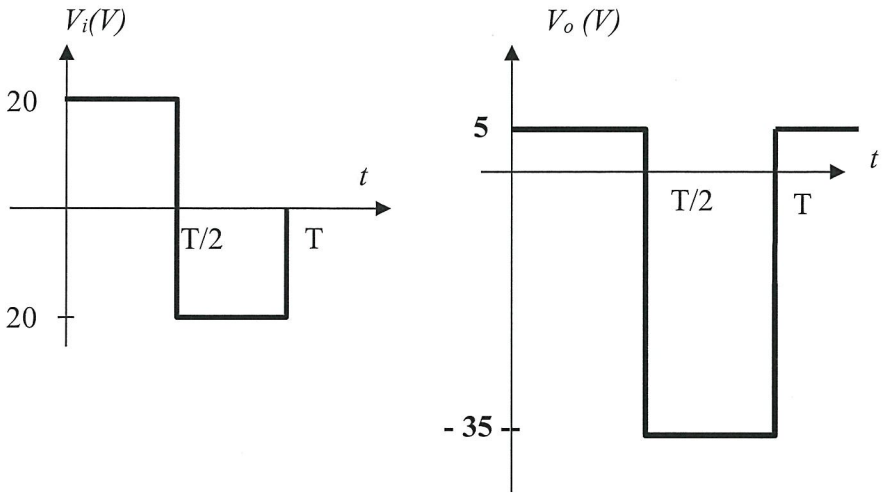

Figure Q1(b)

(c) Zener diode is a special type of P-N junction device which operate in its reverse-breakdown region. **Figure Q1(c)** shows an application of Zener diode in a voltage regulator circuit. Given V_{IN} = 50 V, R = 1 kΩ, V_Z = 10 V and I_{ZM} = 32 mA.

(i) Analyze the range of load resistance, R_L and load current, I_L that will result in V_{RL} being maintained at 10 V.

(7 marks)

(ii) Determine the maximum power rating P_{Zmax} of the Zener diode.

(2 marks)

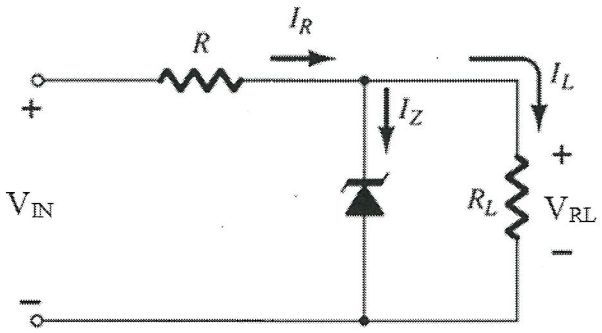

Figure Q1(c)

Q2 (a) **Figure Q2(a)** shows a Bipolar Junction Transistor (BJT) amplifier circuit in voltage – divider configuration. Given the values of $R_1 = 32\ k\Omega$, $R_2 = 3.2\ k\Omega$, $R_C = 10\ k\Omega$, $R_E = 1.5\ k\Omega$, $\beta = 100$ and $V_{CC} = 22$ V. Clearly show all the calculation.

(i) Suppose the circuit is to be analyzed using approximation method. Verify the condition that need to be met.

(1 mark)

(ii) Determine the collector current, I_C of the circuit in **Figure Q2(a)** using exact analysis method.

(7 marks)

(iii) By using the answer from **Q2(a)(ii)**, calculate the dc biasing voltage, V_{CE}.

(2 marks)

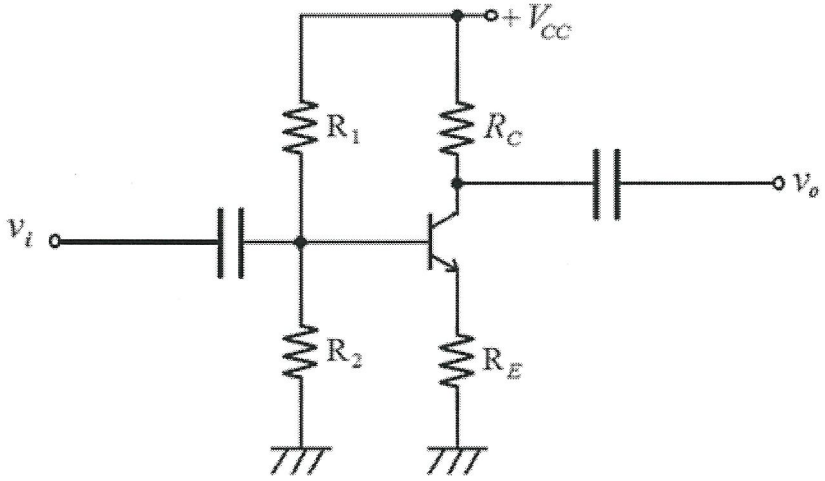

Figure Q2(a)

(b) A common emitter amplifier fixed bias circuit is shown in **Figure Q2(b)**. Given $R_1 = 480\ k\Omega$, $R_C = 3.9\ k\Omega$, $\beta = 200$, $V_{CC} = 15$ V, $C_1 = C_2 = 10\ \mu F$, and assume $V_{BE} = 0.7$ V. Show all the calculation clearly.

(i) Identify the purpose of coupling capacitor in **Figure Q2(b)**.

(2 marks)

(ii) Draw the AC equivalent circuit using r_e model. Assume $r_o = \infty$

(3 marks)

(iii) Calculate the input impedance, Z_i and output impedance, Z_o. (Hint: Check the testing condition and relates with DC analysis if required)

(6 marks)

(iv) Find the voltage gain, A_v and the current gain, A_i.

(4 marks)

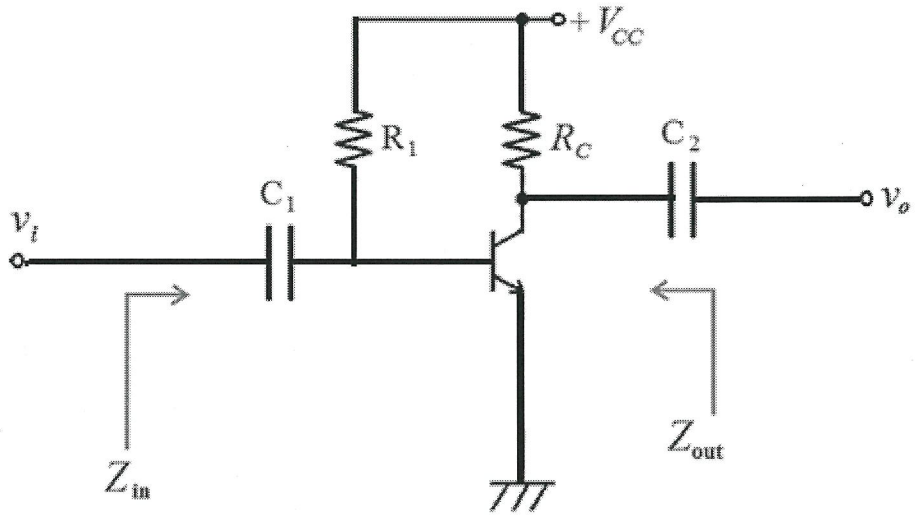

Figure Q2(b)

Q3 (a) The MOSFET (Metal Oxide Semiconductor Field-Effect Transistor) differs from the JFET because it has no PN junction structure. State **TWO (2)** types of MOSFET and briefly explain the operating mode of current and voltage.

(6 marks)

(b) An FET transistor circuit has the following parameters: V_{DD} = 15 V, $R_{G1(UPPER)}$ = 4.7 MΩ, $R_{G2(LOWER)}$ = 3.3 MΩ, R_D = 200 Ω, R_L = 500 Ω, C_g = 1 μF, C_d = 10 μF and C_l = 22 μF. The FET transistor has V_{TH} = 4 V and $I_{D\,(on)}$ = 14 mA at V_{GS} = 6 V.

(i) Draw the FET circuit based on the given parameters.

(1 mark)

(ii) Determine the I_{DQ} and V_{GSQ}.

(3 marks)

(iii) Construct the small-signal equivalent circuit based on the FET transistor circuit drawn in **Q3(b)(i)**.

(3 marks)

(iv) Calculate the input impedance, Z_i, the voltage gain, A_V, the current gain, A_i and the power gain, A_p of the circuit.

(10 marks)

(v) Deduce the effect to the voltage gain, A_v if an additional resistor is connected between source terminal and ground.

(2 marks)

Q4 (a) A common emitter (CE) amplifier shown in **Figure Q4(a)**. The parameters are given as follows:

$V_{CC} = 20$ V $C_S = 10$ µF $C_E = 20$ µF $C_C = 1$ µF $\beta = 100$ $r_o = \infty$ $r_e = 15.76\ \Omega$
$R_S = 1$ kΩ $R_1 = 40$ kΩ $R_2 = 10$ kΩ $R_E = 2$ kΩ $R_C = 4$ kΩ $R_L = 2.2$ kΩ

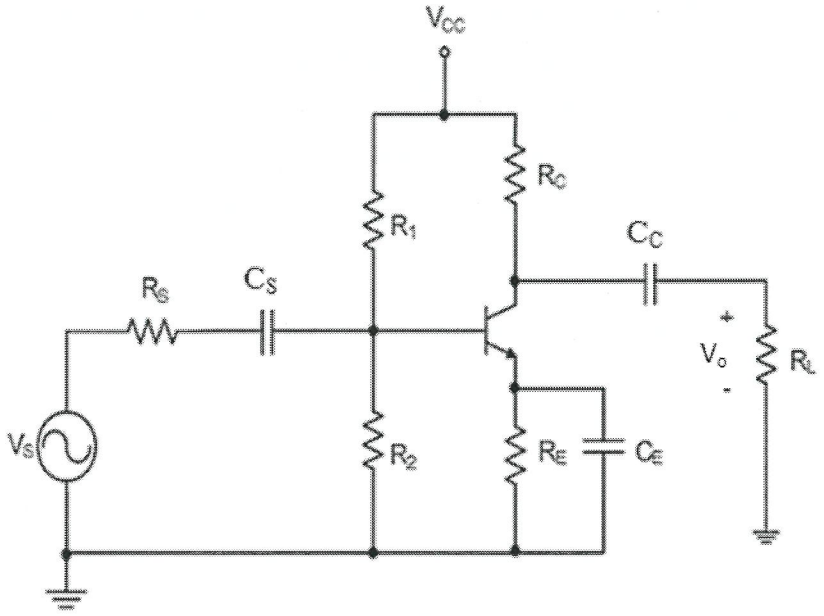

Figure Q4(a)

(i) Determine the cut off frequency due to C_S.

(3 marks)

(ii) Determine the cut off frequency due to C_C.

(3 marks)

(iii) Determine the cut off frequency due to C_E.

(4 marks)

(iv) Draw the resultant frequency response and label clearly the low cut off frequency.

(5 marks)

(b) **Figure Q4(b)** shows a commonly used *Push-Pull* amplifier circuit.

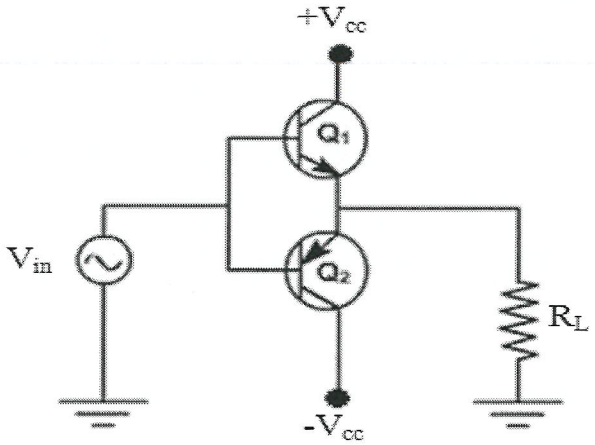

Figure Q4(b)

(i) Explain the operation of the amplifier in **Figure Q4(b)** during positive half cycle and negative half cycle by stating the operation for both Q_1 and Q_2, and the condition of current, I_C.

(4 marks)

(ii) Suppose no bias voltage is applied at both emitter terminals. Redraw the circuit in **Figure Q4(b)** to fulfil this requirement. Name your circuit as **Figure A**.

(1 mark)

(iii) A severe output signal distortion will be resulted due to circuit connections given in **Figure A**. By using a suitable diagram, explain how this problem occurs.

(4 marks)

(iv) Recommend a solution for the problem stated in **Q4(b)(iii)**.

(1 mark)

-END OF QUESTIONS-