

CONFIDENTIAL



UTHM
Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

**FINAL EXAMINATION
SEMESTER II
SESSION 2016/2017**

COURSE NAME : DIGITAL TECHNIQUES

COURSE CODE : BEF 12302

PROGRAMME CODE : BEV

EXAMINATION DATE : JUNE 2017

DURATION : 2 HOURS

**INSTRUCTION : 1. ANSWER ALL QUESTIONS
2. ATTACH APPENDIX A AND B WITH
YOUR ANSWER BOOKLET**

TERBUKA

THIS QUESTION PAPER CONSISTS OF ELEVEN (11) PAGES

CONFIDENTIAL

Q1 (a) List **four (4)** disadvantages of digital system.

(4 marks)

(b) Assuming that all numbers can be represented using 8-bit binary, complete the missing entries which are not shaded in the **Table Q1(b)**. (No mark will be given for this question unless all the solutions are shown).

(8 marks)

(c) American Standard Code for Information Interchange (ASCII) is a character encoding standard which represent text in computers, telecommunications equipment, and other devices. What are the real bit that are send by a computer with a message TRY, using ASCII with odd parity? The ASCII table is given in **Table Q1(c)**.

(6 marks)

(d) A 4-bit binary number is represent by $A_3 A_2 A_1 A_0$ with $A_3 A_2 A_1$ and A_0 are the individual bits and A_0 is the LSB. Draw a minimal combinational logic circuit which produce these two conditions:

(i) An output is HIGH when the $A_3 A_2 A_1 A_0$ should be at least 1_{10} and above and less than 8_{10} .

(ii) An output can be either HIGH or LOW when $A_3 A_2 A_1 A_0$ are 12_{10} and 13_{10} .

(7 marks)

TERBUKA

- Q2** (a) By using De Morgan Theorem, simplify the Boolean expression for Z in **Figure Q2(a)**. (5 marks)
- (b) **Table Q2(b)** shows a truth table of a four-input and two-output logic function. Use Karnaugh maps, formulate:
- (i) The minimal sum-of-product (MSOP) of expression for Y. (5 marks)
- (ii) The minimal product-of-sum (MPOS) of expression for Z. (5 marks)
- (c) A NAND gate is known as a universal gate as it can be configured into any basic logic gate.
- (i) Illustrate how a NAND gate can be used as NOR gate. (3 marks)
- (ii) Implement the function $Z = \overline{\overline{A}B} + \overline{D} + \overline{BC}$ using only a 2-input NAND gates. (7 marks)

TERBUKA

Q3 (a) Explain the operation of the following functional combinational logic circuit. You may use appropriate diagram to aid your explanation.

(i) Encoder. (2 marks)

(ii) Demultiplexer. (2 marks)

(b) Analyze the 8 inputs multiplexer shown in **Figure Q3(b)**.

(i) Draw the truth table. (4 marks)

(ii) Find the simplest Boolean expression for the output Z. (3 marks)

(c) Implement the following Boolean expression using IC 74LS138 (3-to-8 decoder) in **APPENDIX A**. Symbol for IC 74LS138 is shown in **APPENDIX A** for the internal circuitry and pins assignment of 74LS138 (3-to-8 decoder).

$$Z = \overline{\overline{A} + \overline{BC}}$$

(8 marks)

(d) Analyze the flip-flop circuit in **Figure Q3(d)** and sketch output waveform. Complete the timing diagram for Q in **APPENDIX B** and assume that initially Q=0.

(6 marks)

TERBUKA

- Q4** (a) Explain **one (1)** advantage and **two (2)** disadvantages of a synchronous counter compared to asynchronous counter. (3 marks)
- (b) Explain the difference between Moore and Mealy state machine. (4 marks)
- (c) Design a synchronous counter that counts in the sequence of 000, 010, 101, 110 and repeat. The undesired states 001, 011, 100, and 111 must always go to 000 on the NEXT clock pulse. Include in your solutions with:
- (i) State transition diagram. (1 mark)
- (ii) The excitation table for this state machine. Use JK flip flops. (6 marks)
- (iii) The simplest Boolean expression for the circuit using Karnaugh map. (6 marks)
- (iv) Circuit to implement the design. (3 marks)
- (d) Explain the operation of the Serial In Parallel Out register (PISO) register. You may use appropriate diagram to aid your explanation. (2 marks)

- END OF QUESTIONS-

TERBUKA

FINAL EXAMINATION

SEMESTER/SESSION: SEM II/2016/2017
 COURSE : DIGITAL TECHNIQUES

PROGRAMME CODE: BEV
 COURSE CODE : BEF12302

Table Q1(b) : Set numbers in numerical representation

	Binary	Hexadecimal	Unsigned Decimal	Signed Decimal	Gray
Set number 1	?		81		?
Set number 2		D4	?	?	

Table Q1(c) : ASCII table

Dec	Hx	Oct	Char	Dec	Hx	Oct	Chr	Dec	Hx	Oct	Chr	Dec	Hx	Oct	Chr
0	0	000	NUL (null)	32	20	040	Space	64	40	100	@	96	60	140	`
1	1	001	SOH (start of heading)	33	21	041	!	65	41	101	A	97	61	141	a
2	2	002	STX (start of text)	34	22	042	"	66	42	102	B	98	62	142	b
3	3	003	ETX (end of text)	35	23	043	#	67	43	103	C	99	63	143	c
4	4	004	EOT (end of transmission)	36	24	044	\$	68	44	104	D	100	64	144	d
5	5	005	ENQ (enquiry)	37	25	045	%	69	45	105	E	101	65	145	e
6	6	006	ACK (acknowledge)	38	26	046	&	70	46	106	F	102	66	146	f
7	7	007	BEL (bell)	39	27	047	'	71	47	107	G	103	67	147	g
8	8	010	BS (backspace)	40	28	050	(72	48	110	H	104	68	150	h
9	9	011	TAB (horizontal tab)	41	29	051)	73	49	111	I	105	69	151	i
10	A	012	LF (NL line feed, new line)	42	2A	052	*	74	4A	112	J	106	6A	152	j
11	B	013	VT (vertical tab)	43	2B	053	+	75	4B	113	K	107	6B	153	k
12	C	014	FF (NP form feed, newpage)	44	2C	054	,	76	4C	114	L	108	6C	154	l
13	D	015	CR (carriage return)	45	2D	055	-	77	4D	115	M	109	6D	155	m
14	E	016	SO (shift out)	46	2E	056	.	78	4E	116	N	110	6E	156	n
15	F	017	SI (shift in)	47	2F	057	/	79	4F	117	O	111	6F	157	o
16	10	020	DLE (data link escape)	48	30	060	0	80	50	120	P	112	70	160	p
17	11	021	DC1 (device control 1)	49	31	061	1	81	51	121	Q	113	71	161	q
18	12	022	DC2 (device control 2)	50	32	062	2	82	52	122	R	114	72	162	r
19	13	023	DC3 (device control 3)	51	33	063	3	83	53	123	S	115	73	163	s
20	14	024	DC4 (device control 4)	52	34	064	4	84	54	124	T	116	74	164	t
21	15	025	NAK (negative acknowledge)	53	35	065	5	85	55	125	U	117	75	165	u
22	16	026	SYN (synchronous idle)	54	36	066	6	86	56	126	V	118	76	166	v
23	17	027	ETB (end of trans. block)	55	37	067	7	87	57	127	W	119	77	167	w
24	18	030	CAN (cancel)	56	38	070	8	88	58	130	X	120	78	170	x
25	19	031	EM (end of medium)	57	39	071	9	89	59	131	Y	121	79	171	y
26	1A	032	SUB (substitute)	58	3A	072	:	90	5A	132	Z	122	7A	172	z
27	1B	033	ESC (escape)	59	3B	073	;	91	5B	133	[123	7B	173	{
28	1C	034	FS (file separator)	60	3C	074	<	92	5C	134	\	124	7C	174	
29	1D	035	GS (group separator)	61	3D	075	=	93	5D	135]	125	7D	175	}
30	1E	036	RS (record separator)	62	3E	076	>	94	5E	136	^	126	7E	176	~
31	1F	037	US (unit separator)	63	3F	077	?	95	5F	137	_	127	7F	177	DEL

TERBUKA

FINAL EXAMINATION

SEMESTER/SESSION: SEM II/2016/2017
 COURSE :DIGITAL TECHNIQUES

PROGRAMME CODE: BEV
 COURSE CODE : BEF12302

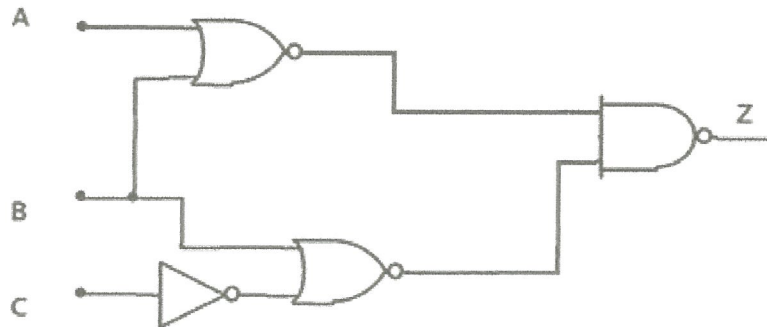


Figure Q2(a)

Table Q2(b)

INPUT				OUTPUT	
A	B	C	D	Y	Z
0	0	0	0	1	0
0	0	0	1	1	1
0	0	1	0	1	X
0	0	1	1	0	X
0	1	0	0	X	1
0	1	0	1	0	0
0	1	1	0	0	1
0	1	1	1	0	1
1	0	0	0	1	0
1	0	0	1	X	1
1	0	1	0	0	X
1	0	1	1	0	1
1	1	0	0	1	1
1	1	0	1	0	X
1	1	1	0	0	0
1	1	1	1	X	0

TERBUKA

FINAL EXAMINATION

SEMESTER/SESSION: SEM II/2016/2017
COURSE :DIGITAL TECHNIQUES

PROGRAMME CODE: BEV
COURSE CODE : BEF12302

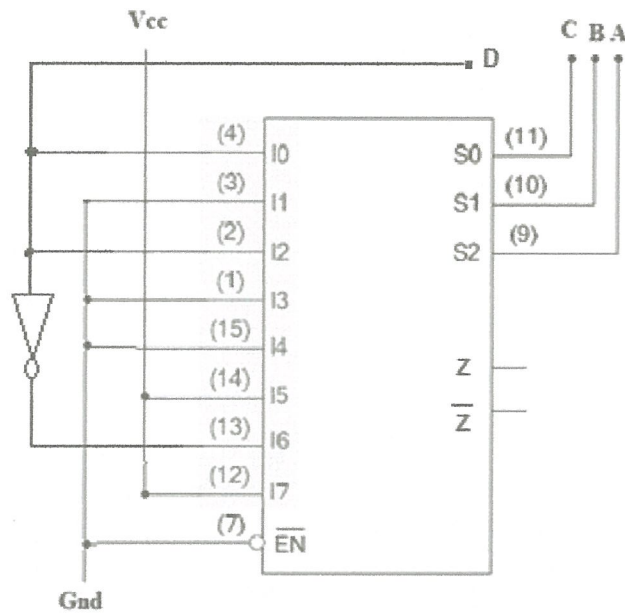


Figure Q3(b)

TERBUKA

FINAL EXAMINATION

SEMESTER/SESSION: SEM II/2016/2017
COURSE :DIGITAL TECHNIQUES

PROGRAMME CODE: BEV
COURSE CODE : BEF12302

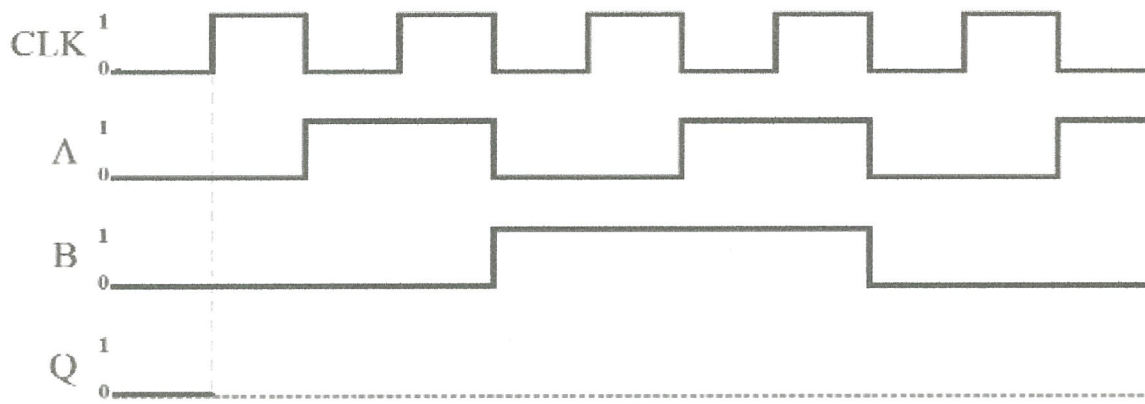
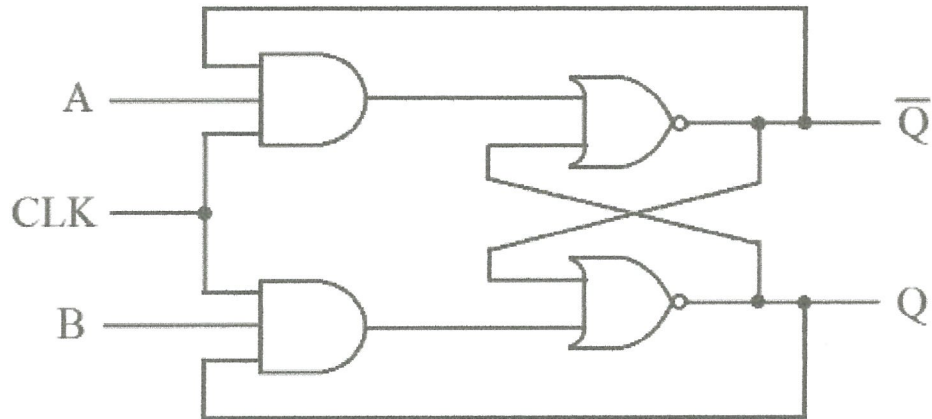


Figure Q3(d)

TERBUKA

FINAL EXAMINATION

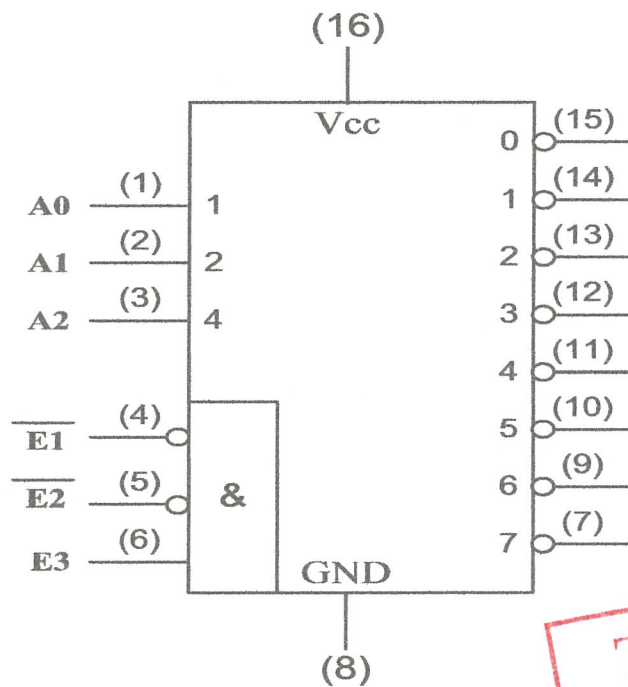
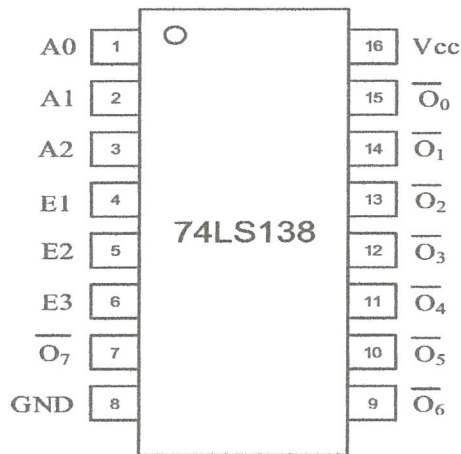
SEMESTER/SESSION: SEM II/2016/2017
COURSE : DIGITAL TECHNIQUES

PROGRAMME CODE: BEV
COURSE CODE : BEF12302

APPENDIX A

PIN ASSIGNMENT AND INTERNAL CIRCUITRY

74LS138 (3-to-8 Decoder)



TERBUKA

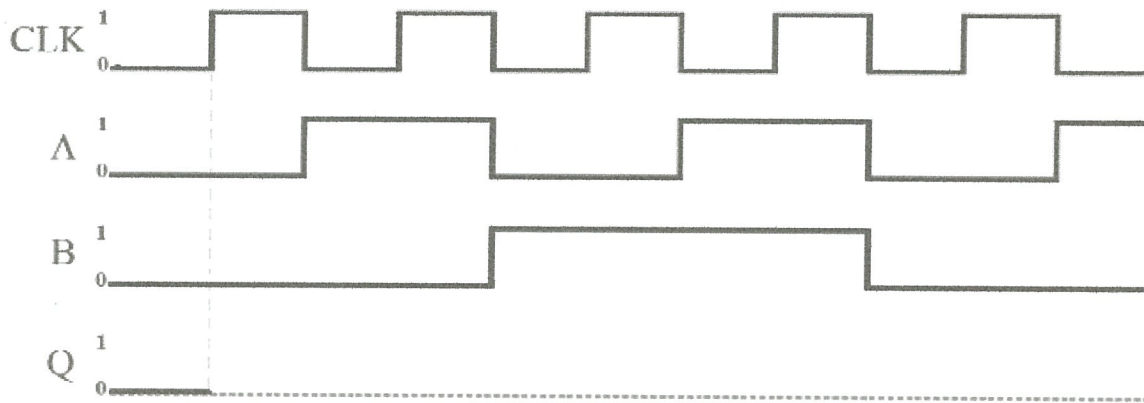
DR. NOR AINIA BINTI SAMRAN
Fakulti Kejuruteraan Elektronik, Kolej
Teknik A. Dinandam, Institut Teknologi
Universiti Tun Hussein Onn Malaysia

FINAL EXAMINATION

SEMESTER/SESSION: SEM II/2016/2017
COURSE :DIGITAL TECHNIQUES

PROGRAMME CODE: BEV
COURSE CODE : BEF12302

APPENDIX B



TERBUKA