Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2016/2017

COURSE NAME	:	DIGITAL IC DESIGN
COURSE CODE	:	BED 30203
PROGRAMME	:	BEJ
EXAMINATION DATE	:	JUNE 2017
DURATION	:	3 HOURS
INSTRUCTION	:	ANSWER **ALL** QUESTIONS

THIS QUESTION PAPER CONSISTS OF **FOUR (4)** PAGES

Q1 (a) The design process of digital integrated circuit is done manually before moving to automated process. Describe the main reason to introduce the automated process.

(4 marks)

(b) Scaling process leads to thinner oxide layer in MOS transistor. Analyse **TWO (2)** reason this phenomenon is less desirable in transistor operation.

(5 marks)

(c) Explain briefly the relation between the length of CMOS transistor and the performance of the device.

(4 marks)

(d) Before implementation of the floorplan, plan how you could arrange the layout of power lines by identifying **TWO (2)** important requirements to ensure the reliability of chip.

(6 marks)

(e) Examine the circuit shown in **Figure Q1(e)** and derive the Boolean equation for node X and output F. For the circuit, the power supply VDD is considered as logic 1.

(6 marks)

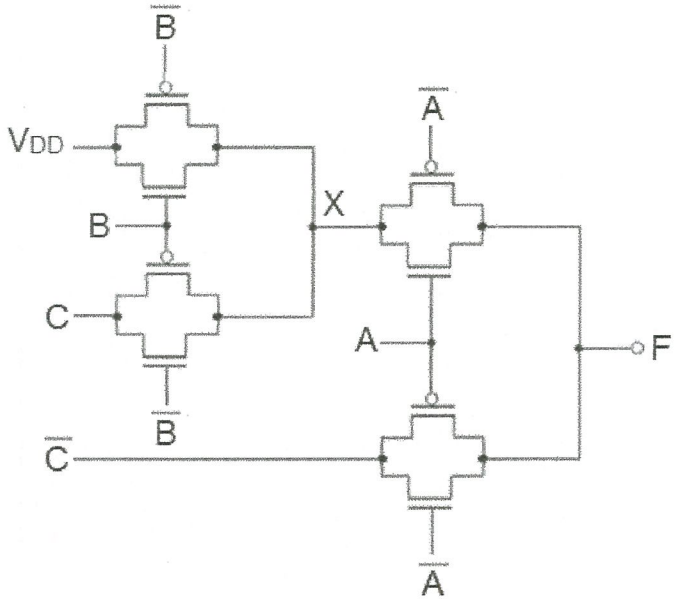

Figure Q1(e)

Q2 A Locomotive Train has 4 active-LOW failsafe sensors. The Train should keep moving unless any of the following conditions arise:

- If the first sensor is activated because the emergency stop button is pressed.
- If engine sensor 2 and engine sensor 3 are activated at the same time.
- If track sensor 4 and engine sensor 3 are activated at the same time.
- If sensors 2, 3, 4 are activated at the same time.

To stop the train, signal HIGH must be generated at the output, Z.

(a) Develop the truth table and acquire the minimum Boolean expression for Z.
(10 marks)

(b) Design a complete transistor-level circuit diagram to realize the equation obtained in **Q2(a)** using a fully complementary static CMOS logic with minimum number of transistor. Assume that all inverted inputs are available. Clearly label the designed circuit.
(8 marks)

(c) Propose the most compact stick diagram layout circuit in **Q2(b)**. Draw and completely label the stick diagram.
(7 marks)

Q3 (a) Predict **TWO (2)** effects on CMOS transistors if they are exposed to electrostatic discharge (ESD).
(6 marks)

(b) Discuss the purpose of wire bonding in chip packaging.
(3 marks)

(c) ASIC is known as a semiconductor circuits specifically designed to suit particular purpose. Explain **TWO (2)** advantages and **TWO (2)** drawbacks of ASIC design flow approach.
(8 marks)

(d) Clock generator cell is a cell to amplify clock signal around the chip with as little delay as possible. It also one of the highest speed signals and may generate a significant amount of noise. Elaborate on the special layout techniques for clock generator cells so it can be implemented effectively.
(8 marks)

Q4 (a) Mismatch between wire size and amount of current flow for power line is one of major concern in layout design. Determine an appropriate approach in power line design that can prevent this problem.

(4 marks)

(b) Power estimation of each block is one of the essential stage in layout design process to estimate the minimum size of the supply lines that will meet the block's requirements. One of the estimation approach is to base on reviewing a previous design. Analyse **FIVE (5)** parameters that you will review from the previous data.

(10 marks)

(c) Besides the power supply routing, it is also important to plan for the clock signal routing. The goal of implementing a clock signal is to distribute a single signal around a large area with minimum delay. Propose **TWO (2)** steps in designing layout for clock generator cell.

(7 marks)

(d) In layout design, there is a compromise between delay minimisation and clock signal optimisation. Propose a suitable method of clock signal design that put more emphasis to reduce delay.

(4 marks)

- END OF QUESTIONS -