Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2016/2017

COURSE NAME	:	DIGITAL ELECTRONICS
COURSE CODE	:	BEL 20303
PROGRAMME	:	BEV/ BEJ
EXAMINATION DATE	:	JUNE 2017
DURATION	:	3 HOURS
INSTRUCTION	:	1. ANSWER **ALL** QUESTIONS 2. ATTACH **APPENDIX I, II AND III** WITH YOUR ANSWER BOOKLET 3. **NO CALCULATOR** IS ALLOWED

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THIS QUESTION PAPER CONSISTS OF **NINE (9)** PAGES

Q1 (a) Convert BCD code 0111 0100 0101 0110 to hexadecimal. Show all the steps.

(5 marks)

(b) Simplify the following Boolean expression.

$$J = \overline{(B \oplus (C + \overline{A}))}$$

(5 marks)

(c) Calculate X and Y in the hexadecimal series below.
880, 881, 883, 886, **X**, 88F, **Y**

(4 marks)

(d) Show how the following Boolean expression can be implemented using only a 2 input NAND gate.

$X = \overline{A \bullet B \bullet C}$

(4 marks)

(e) Prove that the multiplexer with connection shown in **Figure Q1(e)** can functions as a parity generator. State the type of parity method realized by this circuit by giving an appropriate digital data.

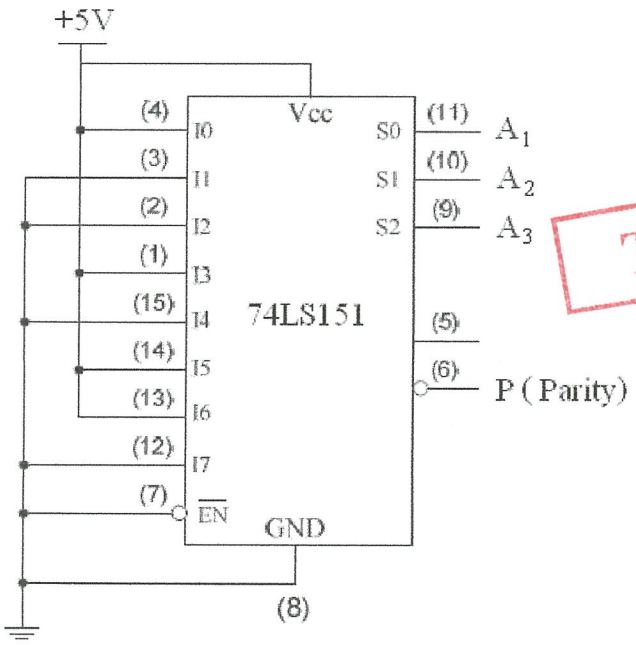

Figure Q1(e)

(7 marks)

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Q2 (a) With the aid of a diagram and truth-table, describe the operation of a 1-to-4 demultiplexer.

(5 marks)

(b) Figure **Q2(b)** shows a 74LS138 decoder that has been constructed to perform a logical operation. Build the truth table of this circuit and determine the Boolean expression for F. There is no need to simplify the Boolean expression.

(6 marks)

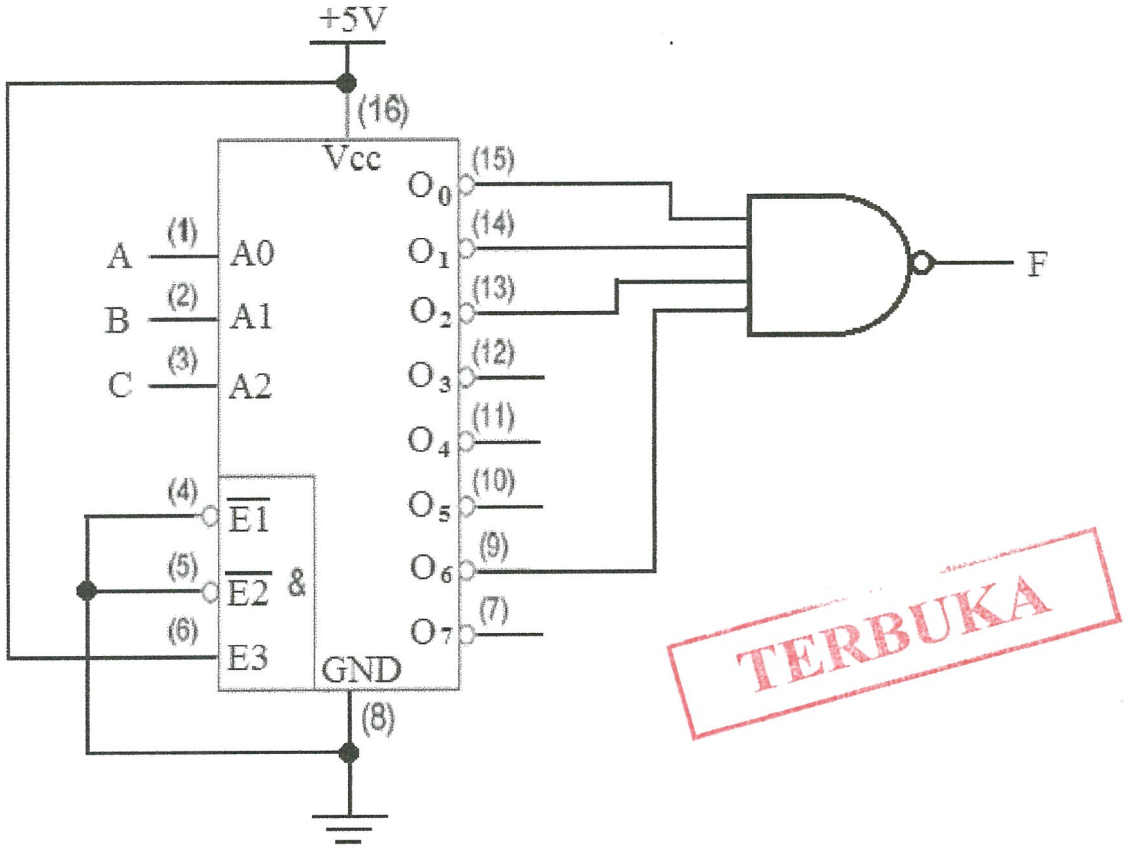

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FIGURE Q2(b)

(c) The input waveforms of signals A and B as shown in **Figure Q2(c)(i)** are applied to the circuit shown in **Figure Q2(b)(ii)**. Simulate with the input waveforms and draw the waveforms for P, Q, R and S in the **APPENDIX I**. Assumes that initially R=0 and S=1.

(8 marks)

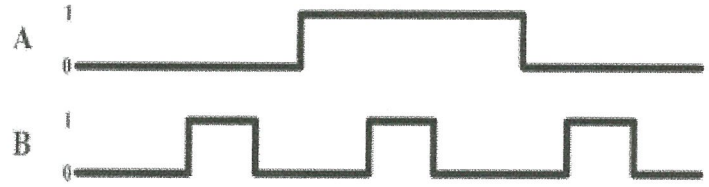

FIGURE Q2(c)(i)

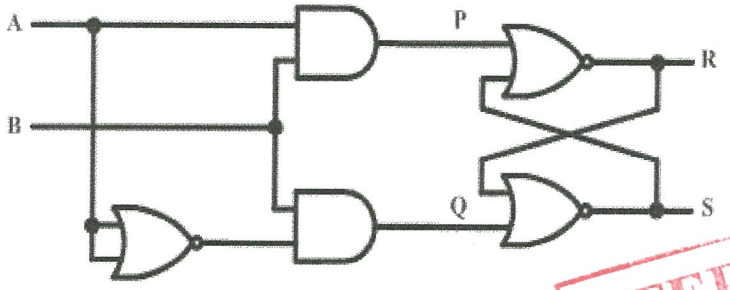

FIGURE Q2(c)(ii)

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(d) Given the circuit diagram of Figure **Q2(c)(i)**, complete the timing diagram for Q_A, Q_B and Q_C in **APPENDIX II**.

(6 marks)

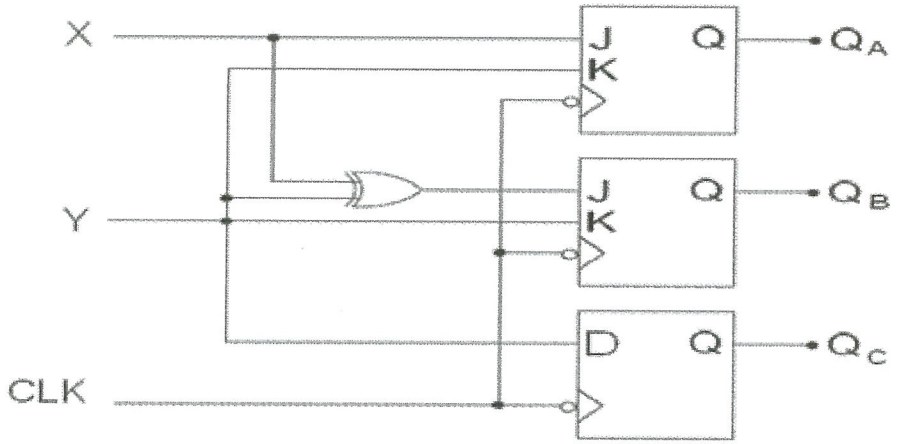

FIGURE Q2(b)(i)

Q3 (a) State the difference between sequential logic circuit and the combinational logic circuit.

(2 marks)

(b) **Figure Q3(b)** shows a 4-bit counter with a specific MOD. MR input is used to reset all flip-flop to LOW. Sketch the timing diagram for Q0, Q1, Q2, Q3, X and Y in the **APPENDIX III**.

(12 marks)

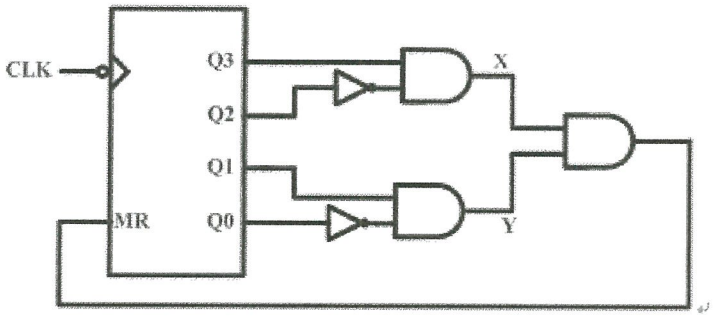

FIGURE Q3(b)

(c) Explain the operation of the following shift register. You may use figure or diagram to aid your explanation.

(i) Serial in/ Parallel out shift register

(3 marks)

(ii) Parallel in/ Serial out shift register

(3 marks)

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(d) Design a circuit that will generate **TWO (2)** frequencies, 12 kHz and 3 kHz at its outputs when a clock signal applied to the circuit is operating at 48 kHz. Use JK flip-flops in your design.

(5 marks)

Q4 A new system of MRT train has **FOUR (4)** active-LOW failure sensors. The Train should keep moving unless any of the following conditions arise:

- If the emergency stop button is pressed the first sensor is activated.
- If engine sensor 2 and engine sensor 3 are activated at the same time.
- If track sensor 4 and engine sensor 3 are activated at the same time.
- If sensors 2,3,4 are activated at the same time.

To stop the train, signal HIGH must be generated at the output, Z.

(a) Derive the truth table for this system.

(12 marks)

(b) Obtain the simplest Boolean expression for Z.

(7 marks)

(c) Draw the complete circuit.

(6 marks)

- END OF QUESTION -

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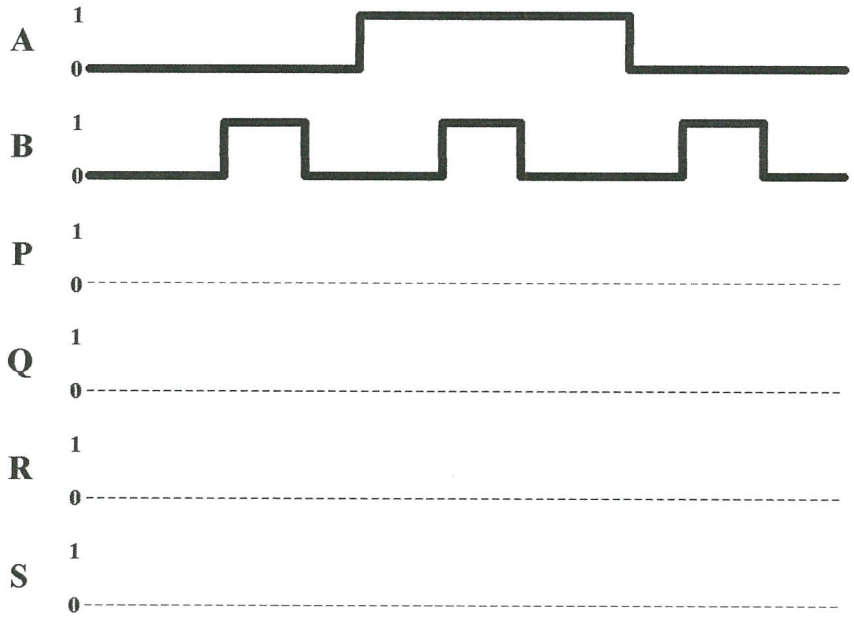
APPENDIX I



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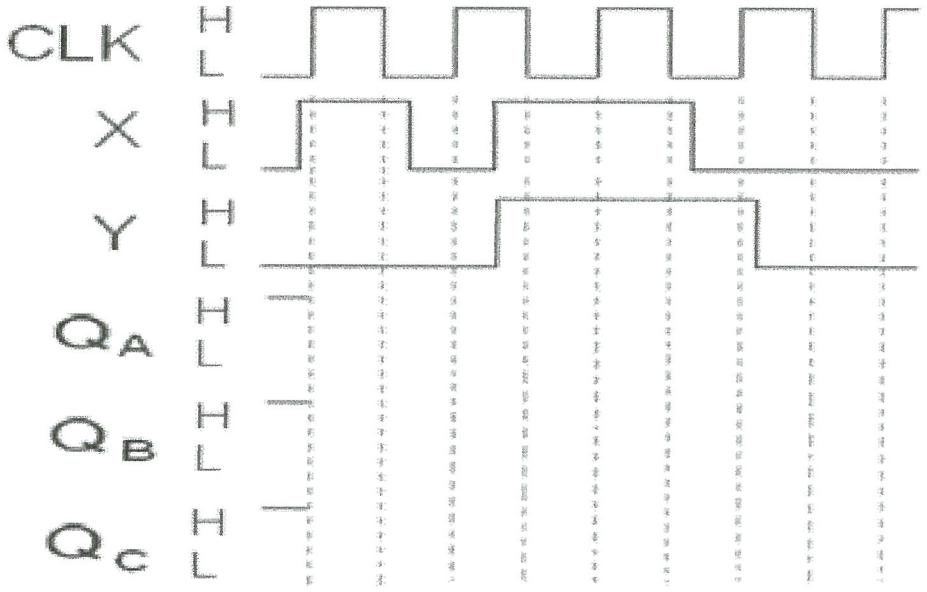
APPENDIX II



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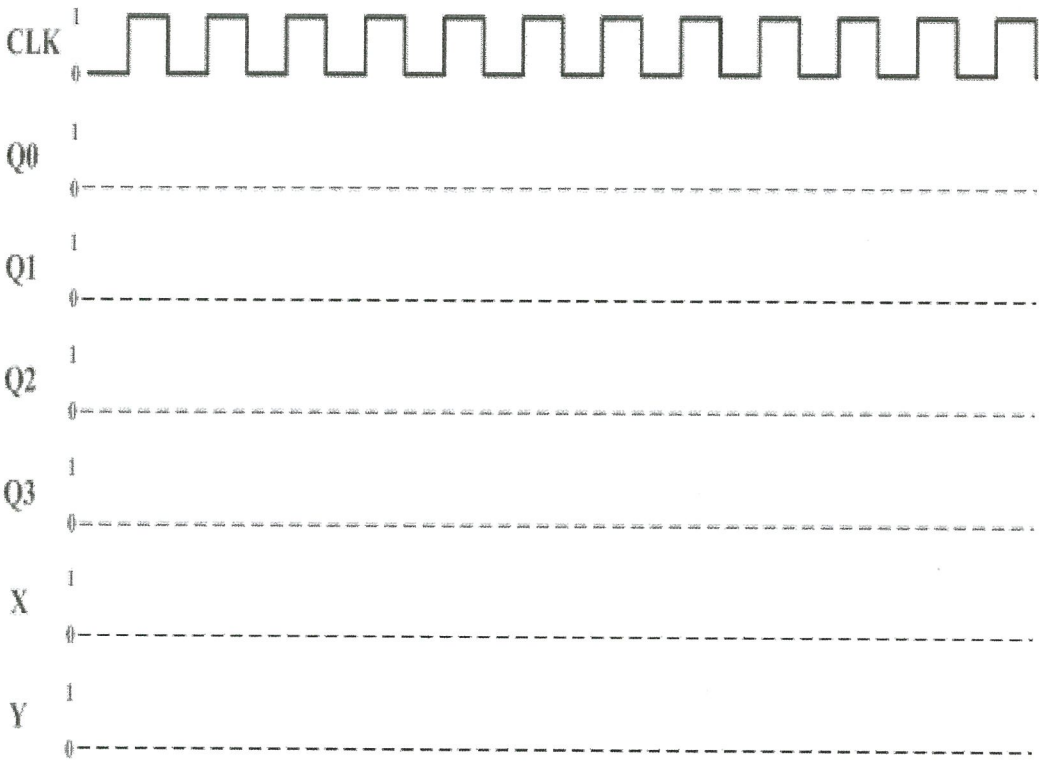
APPENDIX III



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