UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2016/2017

COURSE NAME	:	VLSI DESIGN
COURSE CODE	:	BED 30303
PROGRAMME	:	BEJ
EXAMINATION DATE	:	JUNE 2017
DURATION	:	3 HOURS
INSTRUCTION	:	ANSWER **ALL** QUESTIONS

THIS QUESTION PAPER CONSISTS OF **SIX (6)** PAGES

Q1 (a) Scaling is a very important aspect in VLSI design. Describe and differentiate clearly **THREE (3)** types of scaling in VLSI design.

(6 marks)

(b) **Figure Q1** shows a stick diagram of logical circuit using fully complementary static CMOS.

(i) Analyse the figure and draw the electrically equivalent transistor level schematic of the stick diagram.

(10 marks)

(ii) Determine the logic equation for the output Y.

(4 marks)

Q2 (a) Discuss **ONE (1)** advantage and **ONE (1)** disadvantage of designing a logic circuit at transistor level using dynamic logic method.

(4 marks)

(b) Explain why two dynamic circuits cannot be cascaded together and give **ONE (1)** suggestion on how to eliminate the problem.

(4 marks)

(c) Construct an AND gate at transistor level using transmission gate approach.

(5 marks)

(d) Design a dynamic logic circuit with minimum number of transistors to realize the logic function of $F = \overline{WZ + X(Y + V)}$. The circuit must be able to eliminate a contention problem.

(7 marks)

Q3 (a) List **TWO (2)** sources of leakage current in CMOS transistor and explain clearly the reason why leakage current increases with the advancement of technology scaling in CMOS transistor.

(4 marks)

(b) A logic function is given by equation $Y = \overline{A(B+C)+DE}$

(i) Design a transistor level circuit utilising fully complementary static CMOS logic method to implement the function using minimum number of transistor. The circuit need to have a minimum parasitic delay.

(6 marks)

(ii) Determine the size of each transistor to be used in the design such that the circuit will have an equivalent driving capability of an inverter. Also calculate the minimum parasitic delay. Assume that the minimum length for the transistor is 2λ and the mobility ratio of electron and holes is 2.

(10 marks)

Q4 (a) A negative-level sensitive (negative triggered) D latch circuit can be designed using a circuit as shown in **Figure Q4**.

(i) Obtain the equation for the output of the circuit, Q.

(2 marks)

(ii) Analyse the circuit and determine when the circuit is in 'transparent' form and 'opaque' form with regards to the clock input. Assess the output at these two forms.

(6 marks)

(iii) Modify the circuit to produce a positive-level sensitive (positive triggered) D latch. Draw and clearly label the new circuit and state the new equation for the output.

(4 marks)

(b) Create a positive or rising edge triggered D flip-flop using minimum number of transistors. Draw and completely label the circuit.

(8 marks)

Q5 (a) **Figure Q5(a)** is a block diagram of 2-to-1 multiplexer. Employ a tri-state logic method to implement the multiplexer at transistor level.

(8 marks)

(b) A block diagram of 8-to-3 (octal-to-binary) encoder is shown in **Figure Q5(b)**.

(i) Construct a truth table for the encoder and obtain the equation for each output.

(8 marks)

(ii) Illustrate at transistor level the circuit for the output D_1 of the encoder using dynamic logic with minimum number of transistors.

(4 marks)

– END OF QUESTIONS –

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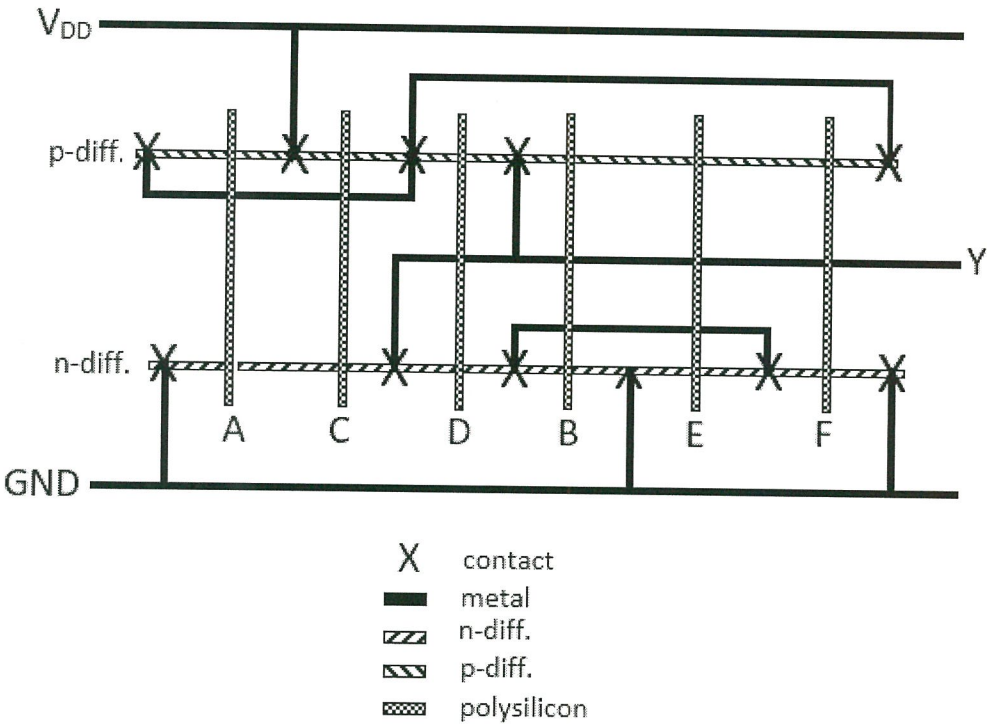

Figure Q1

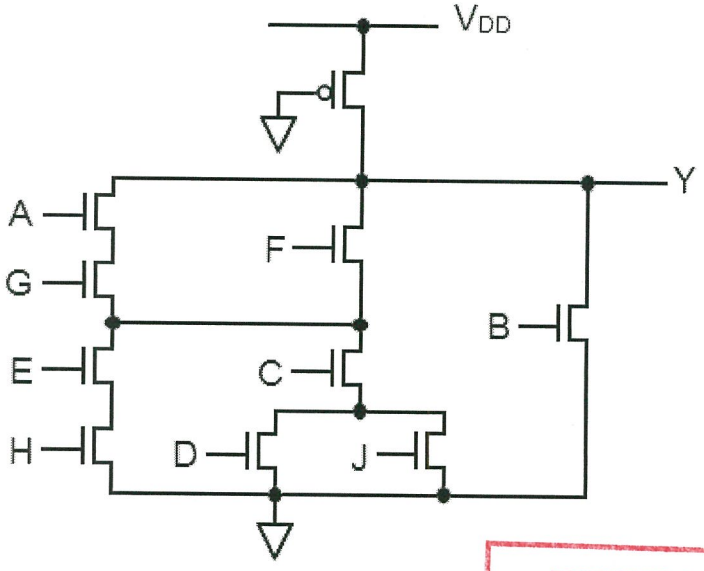

Figure Q2

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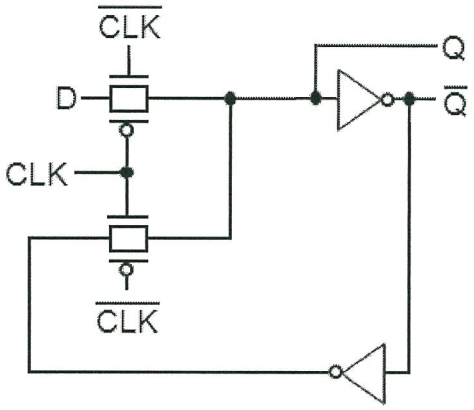

Figure Q4

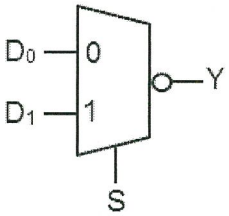

Figure Q5(a)

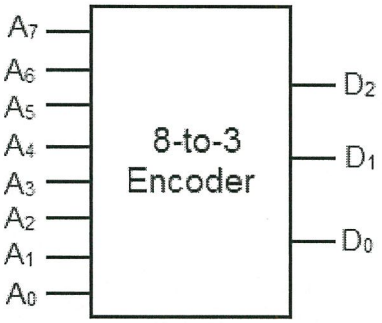

Figure Q5(b)