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**UTHM**  
Universiti Tun Hussein Onn Malaysia

**UNIVERSITI TUN HUSSEIN ONN MALAYSIA**

**FINAL EXAMINATION  
SEMESTER II  
SESSION 2016/2017**

**TERBUKA**

COURSE NAME : MICROPROCESSOR AND  
MICROCONTROLLER

COURSE CODE : BEC 30403

PROGRAMME CODE : BEJ

EXAMINATION DATE : JUNE 2017

DURATION : 3 HOURS

INSTRUCTION : ANSWER ALL QUESTIONS

**THIS QUESTION PAPER CONSISTS OF TWENTY FOUR (24) PAGES**

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Q1 (a) Figure Q1(a) illustrates an ALU unit of the PIC16F877A microcontroller.

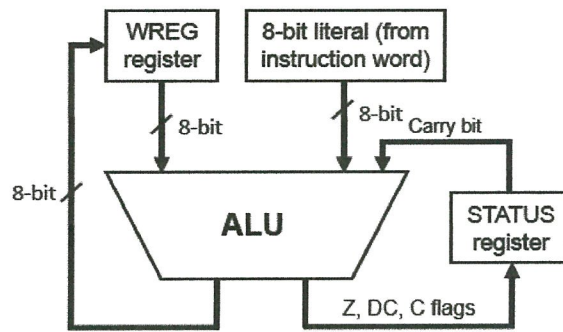


Figure Q1(a)

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By referring to Figure Q1(a), answer the following questions:

- (i) Briefly describe the role of the working (WREG) register in the ALU unit. (2 marks)
- (ii) Explain the maximum value that can be placed in the WREG register. (2 marks)
- (iii) Compare the DC flag bit and C flag bit in Figure Q1(a), justify similarity and the difference between these two bits. (3 marks)
- (iv) Determine the value in WREG register, the status of the C, DC and Z flags after executing the following instructions:

```
MOVLW 0x9C
ADDLW 64H
```

(4 marks)

(b) By referring to Figure Q1(b), answer the following questions:

- (i) Identify bank locations and addresses for PORTB and TRISB Special Function Registers (SFRs). (4 marks)
- (ii) Write a program to initialize lower nibble of PORTB as input pins and upper nibble of PORTB as output pins. (6 marks)
- (iii) With the same configuration as in Q1(b)(ii), determine the value in WREG and PORTB after executing the sequence of instructions below. Justify your answer.

```
MOVLW 0xA4
MOVWF 06H
ADDLW 0x05
```

(4 marks)

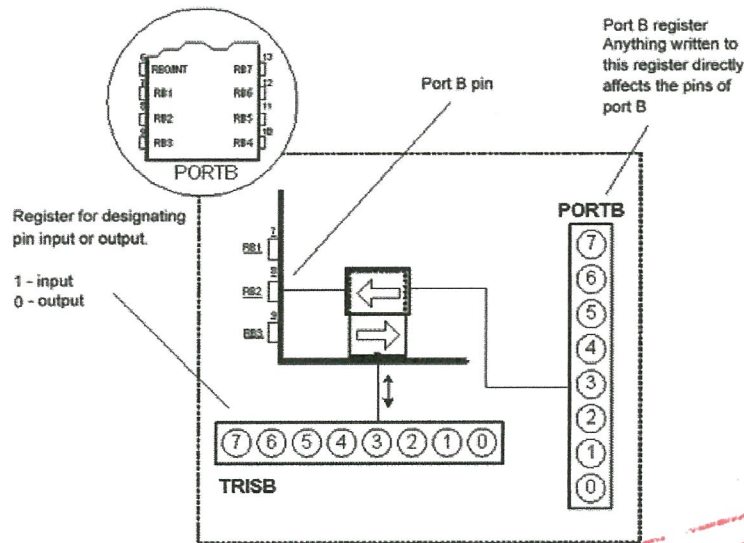


Figure Q1(b)

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- Q2 (a) Interrupt is a very useful mechanism for every microcontroller.
- (i) Explain the process of interrupt in PIC16F877A microcontroller. (4 marks)
  - (ii) Write a sequence of instructions to initialize the interrupt on RB0. The interrupt must be detected on every rising edge of the signal applying to RB0. (4 marks)
  - (iii) Explain why the programmer must clear the interrupt flag bit after every interrupt occurred. (2 marks)
- (b) TMR0 is an 8-bit free run timer of PIC16F877A. Determine the value of OPTION\_REG register if the TMR0 is used as a timer mode. Given the clock speed for the microcontroller is 4MHz and prescaler to be used is dividing by 32. (3 marks)
- (c) **Figure Q2(c)** shows a temperature control system using PIC16F877A microcontroller. A temperature sensor is used to send the temperature in analog voltage to the microcontroller. Based on the temperature reading, the microcontroller controls the heater and the cooler in order to achieve the desired temperature in the plant. At the same time, the temperature data are sent to the computer by using asynchronous serial communication protocol for logging purpose. The PIC is clocked at 4 MHz.

Assume that the desired temperature is between 20°C and 30°C and the value in digital for 20°C is decimal 20 and 30°C is decimal 30.

From the statement above, answer the questions below:

- (i) Construct the flowchart for the microcontroller's program to implement the given system. State the I/O pins in your flowchart. (5 marks)



- (ii) Write a sequence of instruction to initialize the PIC16F877A's USART module by suggesting the suitable values to be used in TXSTA, RCSTA and SPBRG registers respectively if the transfer rate is 9600 baud.

(7 marks)

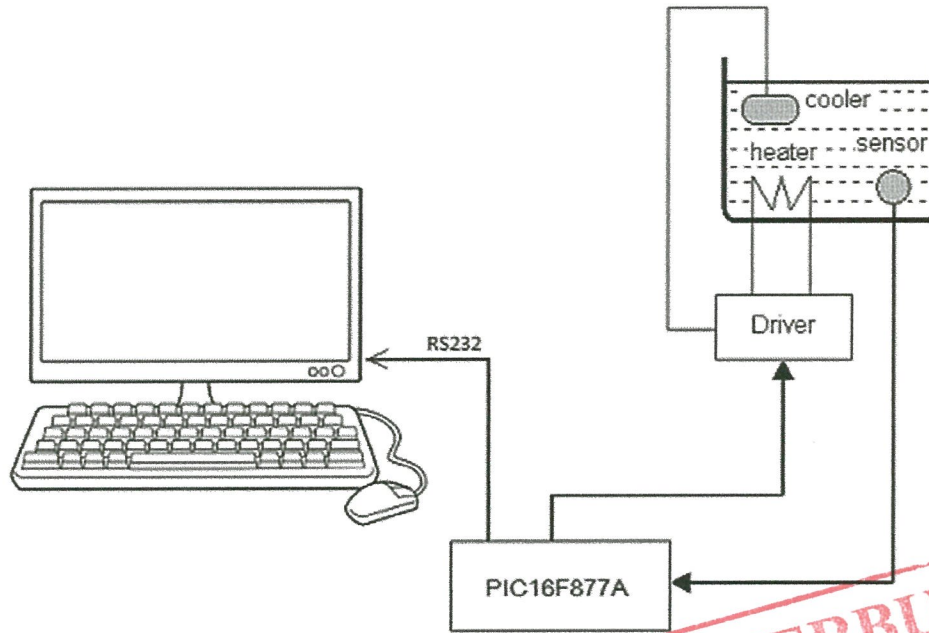


Figure Q2(c)

- Q3 Figure Q3 shows an application using a 4x3 keypad to control the speed of the DC motor using a PWM signal from RC2. When key "1" is pressed, the PWM duty cycle is 0.01 ms, resulting in motor speed of 100 RPM. Table Q3 shows the relation between the keypad, PWM's duty cycle and motor speed. Based on the given specifications, answer the following questions:

- (a) Figure Q3(a) illustrates the signal on pin RC7 when the key "#" is pressed. For the sequence of instruction below, determine which time (whether  $t_1$ ,  $t_2$  or  $t_3$ ) causes the LED to turn ON. Explain your answer.

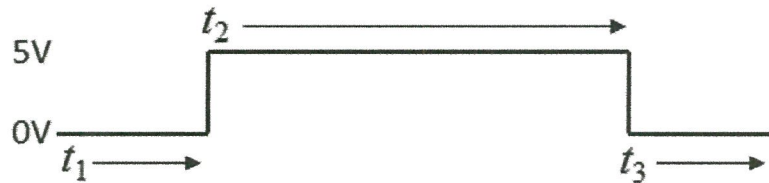


Figure Q3(a)

```

MOV LW    B'00001000'
MOVWF    PORTA
LOOP1    BTFSS    PORTC, 7
         GOTO     LOOP1
LOOP2    BTFSC    PORTC, 7
         GOTO     LOOP2
BSF      PORTD, 0
    
```

(5 marks)



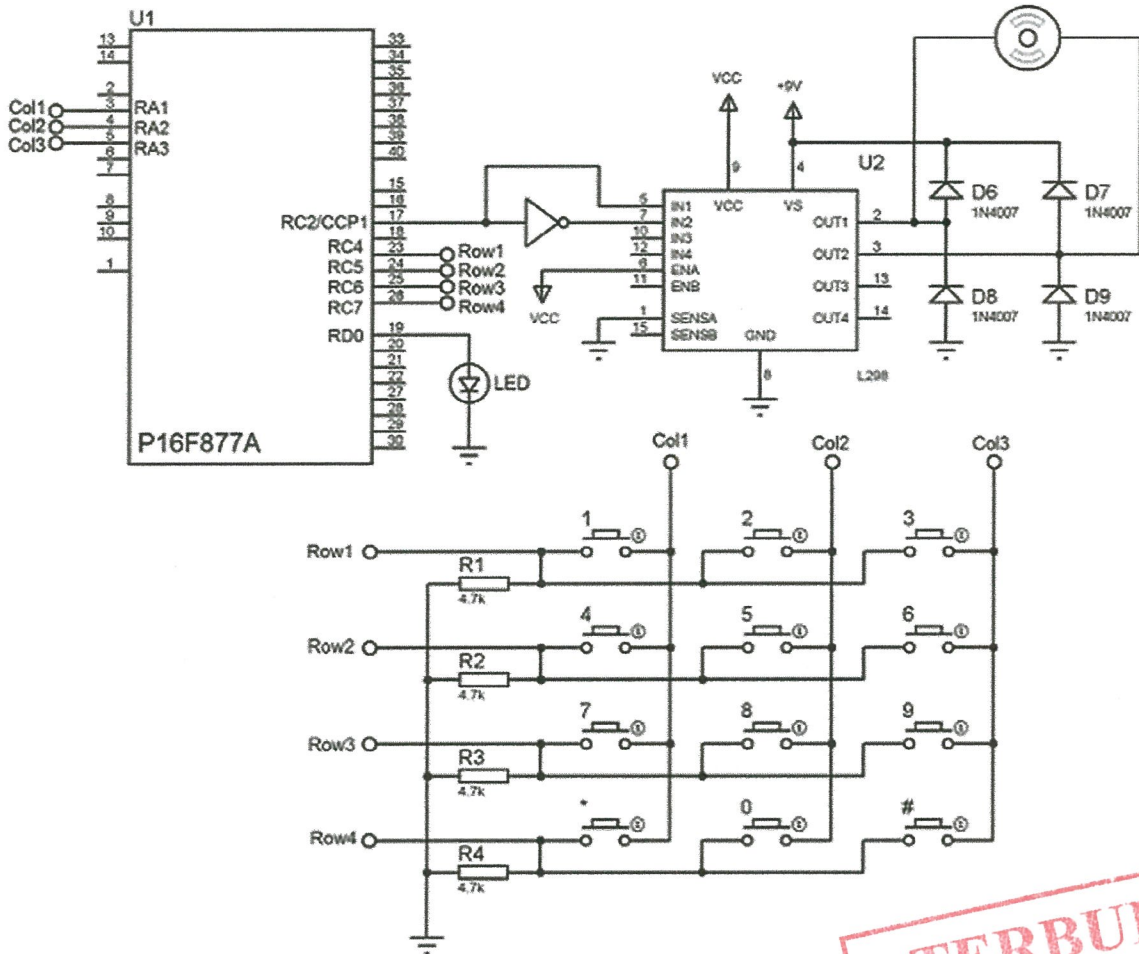


Figure Q3

Table Q3

Key	Speed (RPM)	Duty cycle (ms)
1	100	0.01
2	200	0.02
3	400	0.04

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- (b) Determine the values to be loaded in file register PR2 if the desired PWM frequency is 10 KHz. Furthermore, determine the values in file registers:CCPR1L: CCP1CON<5:4> for the motor speed of 400 RPM. Given TMR2 prescaler = 4. (7 marks)
- (c) Write a sequence of instruction to initialize the PWM module to produce PWM's frequency of 10 KHz. (5 marks)
- (d) Write a sequence of instruction to initialize PORTs that are connected to the keypad. (3 marks)

- (e) If the “interrupt” is to be used for reading the keypad (i.e. the routine for key scan is only activated when the keypad is pressed) suggests the input pins that can be used for this purpose. (2 marks)
- (f) In your opinion, which one is better between using interrupt and not using interrupt (polling) in keypad applications? Justify your answer. (3 marks)

**Q4 (a)** Define microprocessor and what makes it different from microcontroller? (4 marks)

(b) For the 80x86 microprocessor system, show the starting and ending addresses of each segment located by the following segment register values:

- (i) 1000H
- (ii) 1234H
- (iii) 2300H
- (iv) E000H

(2 marks)

(c) Determine the physical address in the memory space of the 80x86 microprocessor for the values in the registers below:

- (i) DS = 1000H and DI = 2000H
- (ii) DS = 2000H and SI = 1002H
- (iii) SS = 2300H and BP = 3200H
- (iv) DS = A000H and BX = 1000H



(2 marks)

(d) Addressing modes are used by a microprocessor to access a particular location within the memory spaces. Write a sequence of instruction to fill in the values of 10H in memory location 0100:1000 to 0100:1200 using register indirect addressing mode. Write comment for each instruction.

(10 marks)

(e) When storing data, one major concern is maintaining data integrity which ensuring that the data retrieved is the same as the data stored. Checksum method is used to detect any data corruption in ROM. For the data in the ROM as follows: 10H, 12H, 30H, 35H, and 20H.

(i) Calculate the checksum byte.

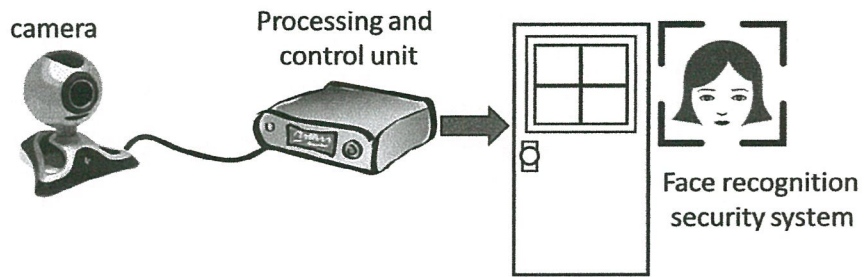
(2 marks)

(ii) Perform the checksum operation to ensure data integrity in the ROM.

(2 marks)

(f) For the security system in **Figure Q4(f)**, suggest a processor to be used (microcontroller / microprocessor) in the “Processing and control unit”. Justify your answer.

(3 marks)



**Figure Q4(f)**

**- END OF QUESTIONS -**

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**FINAL EXAMINATION**

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PROGRAMME : BEJ  
 COURSE CODE : BEC 30403

**PIC16F876A/877A REGISTER FILE MAP**

File Address		File Address		File Address		File Address	
Indirect addr. <sup>(*)</sup>	00h	Indirect addr. <sup>(*)</sup>	80h	Indirect addr. <sup>(*)</sup>	100h	Indirect addr. <sup>(*)</sup>	180h
TMR0	01h	OPTION_REG	81h	TMR0	101h	OPTION_REG	181h
PCL	02h	PCL	82h	PCL	102h	PCL	182h
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTA	05h	TRISA	85h		105h		185h
PORTB	06h	TRISB	86h	PORTB	106h	TRISB	186h
PORTC	07h	TRISC	87h		107h		187h
PORTD <sup>(1)</sup>	08h	TRISD <sup>(1)</sup>	88h		108h		188h
PORTE <sup>(1)</sup>	09h	TRISE <sup>(1)</sup>	89h		109h		189h
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
PIR1	0Ch	PIE1	8Ch	EEDATA	10Ch	EECON1	18Ch
PIR2	0Dh	PIE2	8Dh	EEADR	10Dh	EECON2	18Dh
TMR1L	0Eh	PCON	8Eh	EEDATH	10Eh	Reserved <sup>(2)</sup>	18Eh
TMR1H	0Fh		8Fh	EEADRH	10Fh	Reserved <sup>(2)</sup>	18Fh
T1CON	10h		90h		110h		190h
TMR2	11h	SSPCON2	91h		111h		191h
T2CON	12h	PR2	92h		112h		192h
SSPBUF	13h	SSPADD	93h		113h		193h
SSPCON	14h	SSPSTAT	94h		114h		194h
CCPR1L	15h		95h		115h		195h
CCPR1H	16h		96h		116h		196h
CCP1CON	17h		97h	General Purpose Register 16 Bytes	117h	General Purpose Register 16 Bytes	197h
RCSTA	18h	TXSTA	98h		118h		198h
TXREG	19h	SPBRG	99h		119h		199h
RCREG	1Ah		9Ah		11Ah		19Ah
CCPR2L	1Bh		9Bh		11Bh		19Bh
CCPR2H	1Ch	CMCON	9Ch		11Ch		19Ch
CCP2CON	1Dh	CVRCON	9Dh		11Dh		19Dh
ADRESH	1Eh	ADRESL	9Eh		11Eh		19Eh
ADCON0	1Fh	ADCON1	9Fh		11Fh		19Fh
	20h		A0h		120h		1A0h
General Purpose Register 96 Bytes		General Purpose Register 80 Bytes		General Purpose Register 80 Bytes		General Purpose Register 80 Bytes	
		accesses 70h-7Fh	EFh F0h	accesses 70h-7Fh	16Fh 170h	accesses 70h - 7Fh	1EFh 1F0h
Bank 0	7Fh	Bank 1	FFh	Bank 2	17Fh	Bank 3	1FFh

■ Unimplemented data memory locations, read as '0'.  
 \* Not a physical register.

**Note 1:** These registers are not implemented on the PIC16F876A.  
**Note 2:** These registers are reserved; maintain these registers clear.





**FINAL EXAMINATION**

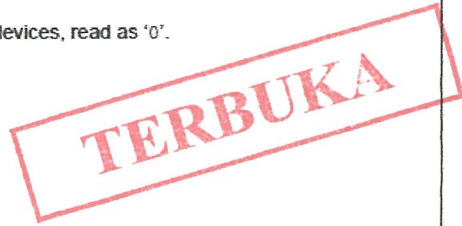
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**SPECIAL FUNCTION REGISTER SUMMARY**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on page:
<b>Bank 0</b>											
00h <sup>(3)</sup>	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	31, 150
01h	TMR0	Timer0 Module Register								xxxx xxxx	55, 150
02h <sup>(3)</sup>	PCL	Program Counter (PC) Least Significant Byte								0000 0000	30, 150
03h <sup>(3)</sup>	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	C	0001 1xxxx	22, 150
04h <sup>(3)</sup>	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	31, 150
05h	PORTA	—	—	PORTA Data Latch when written: PORTA pins when read						--0x 0000	43, 150
06h	PORTB	PORTB Data Latch when written: PORTB pins when read								xxxx xxxxx	45, 150
07h	PORTC	PORTC Data Latch when written: PORTC pins when read								xxxx xxxxx	47, 150
08h <sup>(4)</sup>	PORTD	PORTD Data Latch when written: PORTD pins when read								xxxx xxxxx	48, 150
09h <sup>(4)</sup>	PORTE	—	—	—	—	—	RE2	RE1	RE0	---- -xxxx	49, 150
0Ah <sup>(1,3)</sup>	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	30, 150
0Bh <sup>(3)</sup>	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	24, 150
0Ch	PIR1	PSPIF <sup>(3)</sup>	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	26, 150
0Dh	PIR2	—	CMIF	—	EEIF	BCLIF	—	—	CCP2IF	-0-0 0--0	28, 150
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxxx	60, 150
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxxx	60, 150
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	--00 0000	57, 150
11h	TMR2	Timer2 Module Register								0000 0000	62, 150
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	61, 150
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxxx	79, 150
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	82, 82, 150
15h	CCPR1L	Capture/Compare/PWM Register 1 (LSB)								xxxx xxxxx	63, 150
16h	CCPR1H	Capture/Compare/PWM Register 1 (MSB)								xxxx xxxxx	63, 150
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	64, 150
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	112, 150
19h	TXREG	USART Transmit Data Register								0000 0000	118, 150
1Ah	RCREG	USART Receive Data Register								0000 0000	118, 150
1Bh	CCPR2L	Capture/Compare/PWM Register 2 (LSB)								xxxx xxxxx	63, 150
1Ch	CCPR2H	Capture/Compare/PWM Register 2 (MSB)								xxxx xxxxx	63, 150
1Dh	CCP2CON	—	—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	64, 150
1Eh	ADRESH	A/D Result Register High Byte								xxxx xxxxx	133, 150
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	—	ADON	0000 00-0	127, 150

**Legend:** x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.  
 Shaded locations are unimplemented, read as '0'.  
**Note 1:** The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8>, whose contents are transferred to the upper byte of the program counter.  
**2:** Bits PSPIE and PSPIF are reserved on PIC16F873A/876A devices; always maintain these bits clear.  
**3:** These registers can be addressed from any bank.  
**4:** PORTD, PORTE, TRISD and TRISE are not implemented on PIC16F873A/876A devices, read as '0'.  
**5:** Bit 4 of EEADRH implemented only on the PIC16F876A/877A devices.





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**SPECIAL FUNCTION REGISTER SUMMARY (Continued)**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on page:
<b>Bank 1</b>											
80h <sup>(3)</sup>	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	31, 150
81h	OPTION_REG	R $\overline{\text{BPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	23, 150
82h <sup>(3)</sup>	PCL	Program Counter (PC) Least Significant Byte								0000 0000	30, 150
83h <sup>(3)</sup>	STATUS	IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	22, 150
84h <sup>(3)</sup>	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	31, 150
85h	TRISA	—	—	PORTA Data Direction Register						--11 1111	43, 150
86h	TRISB	PORTB Data Direction Register								1111 1111	45, 150
87h	TRISC	PORTC Data Direction Register								1111 1111	47, 150
88h <sup>(4)</sup>	TRISD	PORTD Data Direction Register								1111 1111	48, 151
89h <sup>(4)</sup>	TRISE	IBF	OBF	IBOV	PSPMODE	—	PORTE Data Direction bits			0000 -111	50, 151
8Ah <sup>(1,3)</sup>	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	30, 150
8Bh <sup>(3)</sup>	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	24, 150
8Ch	PIE1	PSPIE <sup>(2)</sup>	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	25, 151
8Dh	PIE2	—	CMIE	—	EEIE	BCLIE	—	—	CCP2IE	-0-0 0--0	27, 151
8Eh	PCON	—	—	—	—	—	—	POR	BOR	---- --qq	29, 151
8Fh	—	Unimplemented								—	—
90h	—	Unimplemented								—	—
91h	SSPCON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0000 0000	83, 151
92h	PR2	Timer2 Period Register								1111 1111	62, 151
93h	SSPAD	Synchronous Serial Port (I <sup>2</sup> C mode) Address Register								0000 0000	79, 151
94h	SSPSTAT	SMP	CKE	D $\overline{\text{A}}$	P	S	R $\overline{\text{W}}$	UA	BF	0000 0000	79, 151
95h	—	Unimplemented								—	—
96h	—	Unimplemented								—	—
97h	—	Unimplemented								—	—
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	111, 151
99h	SPBRG	Baud Rate Generator Register								0000 0000	113, 151
9Ah	—	Unimplemented								—	—
9Bh	—	Unimplemented								—	—
9Ch	CMCON	C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0111	135, 151
9Dh	CVRCON	CVREN	CVROE	CVRR	—	CVR3	CVR2	CVR1	CVR0	000- 0000	141, 151
9Eh	ADRESL	A/D Result Register Low Byte								xxxx xxxx	133, 151
9Fh	ADCON1	ADFM	ADCS2	—	—	PCFG3	PCFG2	PCFG1	PCFG0	00-- 0000	128, 151

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**SPECIAL FUNCTION REGISTER SUMMARY (Continued)**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on page:
<b>Bank 2</b>											
100h <sup>(3)</sup>	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	31, 150
101h	TMR0	Timer0 Module Register								xxxx xxxx	55, 150
102h <sup>(3)</sup>	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	30, 150
103h <sup>(3)</sup>	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	22, 150
104h <sup>(3)</sup>	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	31, 150
105h	—	Unimplemented								—	—
106h	PORTB	PORTB Data Latch when written: PORTB pins when read								xxxx xxxx	45, 150
107h	—	Unimplemented								—	—
108h	—	Unimplemented								—	—
109h	—	Unimplemented								—	—
10Ah <sup>(1,3)</sup>	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	30, 150
10Bh <sup>(3)</sup>	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	24, 150
10Ch	EEDATA	EEPROM Data Register Low Byte								xxxx xxxx	39, 151
10Dh	EEADR	EEPROM Address Register Low Byte								xxxx xxxx	39, 151
10Eh	EEDATH	—	—	EEPROM Data Register High Byte					--xx xxxx	39, 151	
10Fh	EEADRH	—	—	—	— <sup>(5)</sup>	EEPROM Address Register High Byte				--- xxxx	39, 151
<b>Bank 3</b>											
180h <sup>(3)</sup>	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	31, 150
181h	OPTION_REG	RBPV	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	23, 150
182h <sup>(3)</sup>	PCL	Program Counter (PC) Least Significant Byte								0000 0000	30, 150
183h <sup>(3)</sup>	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	22, 150
184h <sup>(3)</sup>	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	31, 150
185h	—	Unimplemented								—	—
186h	TRISB	PORTB Data Direction Register								1111 1111	45, 150
187h	—	Unimplemented								—	—
188h	—	Unimplemented								—	—
189h	—	Unimplemented								—	—
18Ah <sup>(1,3)</sup>	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	30, 150
18Bh <sup>(3)</sup>	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	24, 150
18Ch	EECON1	EEPGD	—	—	—	WRERR	WREN	WR	RD	x--- x000	34, 151
18Dh	EECON2	EEPROM Control Register 2 (not a physical register)								---- ----	39, 151
18Eh	—	Reserved; maintain clear								0000 0000	—
18Fh	—	Reserved; maintain clear								0000 0000	—

- Legend:** x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.
- Note 1:** The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8>, whose contents are transferred to the upper byte of the program counter.
- 2:** Bits PSPIE and PSPIF are reserved on PIC16F873A/876A devices; always maintain these bits clear.
- 3:** These registers can be addressed from any bank.
- 4:** PORTD, PORTE, TRISD and TRISE are not implemented on PIC16F873A/876A devices, read as '0'.
- 5:** Bit 4 of EEADRH implemented only on the PIC16F876A/877A devices.





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**STATUS REGISTER (ADDRESS 03h, 83h, 103h, 183h)**

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x	
IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	
bit 7								bit 0

bit 7 **IRP:** Register Bank Select bit (used for indirect addressing)

- 1 = Bank 2, 3 (100h-1FFh)
- 0 = Bank 0, 1 (00h-FFh)

bit 6-5 **RP1:RP0:** Register Bank Select bits (used for direct addressing)

- 11 = Bank 3 (180h-1FFh)
- 10 = Bank 2 (100h-17Fh)
- 01 = Bank 1 (80h-FFh)
- 00 = Bank 0 (00h-7Fh)
- Each bank is 128 bytes.

bit 4  **$\overline{TO}$ :** Time-out bit

- 1 = After power-up, CLRWDT instruction or SLEEP instruction
- 0 = A WDT time-out occurred

bit 3  **$\overline{PD}$ :** Power-down bit

- 1 = After power-up or by the CLRWDT instruction
- 0 = By execution of the SLEEP instruction

bit 2 **Z:** Zero bit

- 1 = The result of an arithmetic or logic operation is zero
- 0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit carry/borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)

- (for borrow, the polarity is reversed)
- 1 = A carry-out from the 4th low order bit of the result occurred
- 0 = No carry-out from the 4th low order bit of the result

bit 0 **C:** Carry/borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)

- 1 = A carry-out from the Most Significant bit of the result occurred
- 0 = No carry-out from the Most Significant bit of the result occurred

**Note:** For  $\overline{borrow}$ , the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high, or low order bit of the source register.

<b>Legend:</b>			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown



**FINAL EXAMINATION**

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 COURSE : MICROPROCESSOR AND MICROCONTROLLER

PROGRAMME : BEJ  
 COURSE CODE : BEC 30403

**OPTION\_REG REGISTER (ADDRESS 81h, 181h)**

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
RBP̄U	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7						bit 0	

- bit 7 **RBP̄U**: PORTB Pull-up Enable bit  
 1 = PORTB pull-ups are disabled  
 0 = PORTB pull-ups are enabled by individual port latch values
- bit 6 **INTEDG**: Interrupt Edge Select bit  
 1 = Interrupt on rising edge of RB0/INT pin  
 0 = Interrupt on falling edge of RB0/INT pin
- bit 5 **T0CS**: TMR0 Clock Source Select bit  
 1 = Transition on RA4/T0CKI pin  
 0 = Internal instruction cycle clock (CLKO)
- bit 4 **T0SE**: TMR0 Source Edge Select bit  
 1 = Increment on high-to-low transition on RA4/T0CKI pin  
 0 = Increment on low-to-high transition on RA4/T0CKI pin
- bit 3 **PSA**: Prescaler Assignment bit  
 1 = Prescaler is assigned to the WDT  
 0 = Prescaler is assigned to the Timer0 module
- bit 2-0 **PS2:PS0**: Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

**Legend:**  
 R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 - n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown



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**INTCON REGISTER (ADDRESS 0Bh, 8Bh, 10Bh, 18Bh)**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF
bit 7							bit 0

- bit 7 **GIE:** Global Interrupt Enable bit  
 1 = Enables all unmasked interrupts  
 0 = Disables all interrupts
- bit 6 **PEIE:** Peripheral Interrupt Enable bit  
 1 = Enables all unmasked peripheral interrupts  
 0 = Disables all peripheral interrupts
- bit 5 **TMR0IE:** TMR0 Overflow Interrupt Enable bit  
 1 = Enables the TMR0 interrupt  
 0 = Disables the TMR0 interrupt
- bit 4 **INTE:** RB0/INT External Interrupt Enable bit  
 1 = Enables the RB0/INT external interrupt  
 0 = Disables the RB0/INT external interrupt
- bit 3 **RBIE:** RB Port Change Interrupt Enable bit  
 1 = Enables the RB port change interrupt  
 0 = Disables the RB port change interrupt
- bit 2 **TMR0IF:** TMR0 Overflow Interrupt Flag bit  
 1 = TMR0 register has overflowed (must be cleared in software)  
 0 = TMR0 register did not overflow
- bit 1 **INTF:** RB0/INT External Interrupt Flag bit  
 1 = The RB0/INT external interrupt occurred (must be cleared in software)  
 0 = The RB0/INT external interrupt did not occur
- bit 0 **RBIF:** RB Port Change Interrupt Flag bit  
 1 = At least one of the RB7:RB4 pins changed state; a mismatch condition will continue to set the bit. Reading PORTB will end the mismatch condition and allow the bit to be cleared (must be cleared in software).  
 0 = None of the RB7:RB4 pins have changed state

<b>Legend:</b>			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown



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**PIE1 REGISTER (ADDRESS 8Ch)**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PSPIE <sup>(1)</sup>	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE
bit 7							bit 0

bit 7 **PSPIE:** Parallel Slave Port Read/Write Interrupt Enable bit<sup>(1)</sup>  
 1 = Enables the PSP read/write interrupt  
 0 = Disables the PSP read/write interrupt

**Note 1:** PSPIE is reserved on PIC16F873A/876A devices; always maintain this bit clear.

bit 6 **ADIE:** A/D Converter Interrupt Enable bit  
 1 = Enables the A/D converter interrupt  
 0 = Disables the A/D converter interrupt

bit 5 **RCIE:** USART Receive Interrupt Enable bit  
 1 = Enables the USART receive interrupt  
 0 = Disables the USART receive interrupt

bit 4 **TXIE:** USART Transmit Interrupt Enable bit  
 1 = Enables the USART transmit interrupt  
 0 = Disables the USART transmit interrupt

bit 3 **SSPIE:** Synchronous Serial Port Interrupt Enable bit  
 1 = Enables the SSP interrupt  
 0 = Disables the SSP interrupt

bit 2 **CCP1IE:** CCP1 Interrupt Enable bit  
 1 = Enables the CCP1 interrupt  
 0 = Disables the CCP1 interrupt

bit 1 **TMR2IE:** TMR2 to PR2 Match Interrupt Enable bit  
 1 = Enables the TMR2 to PR2 match interrupt  
 0 = Disables the TMR2 to PR2 match interrupt

bit 0 **TMR1IE:** TMR1 Overflow Interrupt Enable bit  
 1 = Enables the TMR1 overflow interrupt  
 0 = Disables the TMR1 overflow interrupt



<b>Legend:</b>			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

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**PIR1 REGISTER (ADDRESS 0Ch)**

R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
PSPIF <sup>(1)</sup>	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF
bit 7						bit 0	

- bit 7 **PSPIF:** Parallel Slave Port Read/Write Interrupt Flag bit<sup>(1)</sup>  
 1 = A read or a write operation has taken place (must be cleared in software)  
 0 = No read or write has occurred  
**Note 1:** PSPIF is reserved on PIC16F873A/876A devices; always maintain this bit clear.
- bit 6 **ADIF:** A/D Converter Interrupt Flag bit  
 1 = An A/D conversion completed  
 0 = The A/D conversion is not complete
- bit 5 **RCIF:** USART Receive Interrupt Flag bit  
 1 = The USART receive buffer is full  
 0 = The USART receive buffer is empty
- bit 4 **TXIF:** USART Transmit Interrupt Flag bit  
 1 = The USART transmit buffer is empty  
 0 = The USART transmit buffer is full
- bit 3 **SSPIF:** Synchronous Serial Port (SSP) Interrupt Flag bit  
 1 = The SSP interrupt condition has occurred and must be cleared in software before returning from the Interrupt Service Routine. The conditions that will set this bit are:
  - SPI – A transmission/reception has taken place.
  - I<sup>2</sup>C Slave – A transmission/reception has taken place.
  - I<sup>2</sup>C Master
    - A transmission/reception has taken place.
    - The initiated Start condition was completed by the SSP module.
    - The initiated Stop condition was completed by the SSP module.
    - The initiated Restart condition was completed by the SSP module.
    - The initiated Acknowledge condition was completed by the SSP module.
    - A Start condition occurred while the SSP module was Idle (multi-master system).
    - A Stop condition occurred while the SSP module was Idle (multi-master system).
 0 = No SSP interrupt condition has occurred
- bit 2 **CCP1IF:** CCP1 Interrupt Flag bit  
Capture mode:  
 1 = A TMR1 register capture occurred (must be cleared in software)  
 0 = No TMR1 register capture occurred  
Compare mode:  
 1 = A TMR1 register compare match occurred (must be cleared in software)  
 0 = No TMR1 register compare match occurred  
PWM mode:  
 Unused in this mode.
- bit 1 **TMR2IF:** TMR2 to PR2 Match Interrupt Flag bit  
 1 = TMR2 to PR2 match occurred (must be cleared in software)  
 0 = No TMR2 to PR2 match occurred
- bit 0 **TMR1IF:** TMR1 Overflow Interrupt Flag bit  
 1 = TMR1 register overflowed (must be cleared in software)  
 0 = TMR1 register did not overflow

<b>Legend:</b>			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown



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**REGISTERS ASSOCIATED WITH PWM AND TIMER2**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Bh,8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF <sup>(1)</sup>	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
0Dh	PIR2	—	—	—	—	—	—	—	CCP2IF	---- --0	---- --0
8Ch	PIE1	PSPIE <sup>(1)</sup>	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
8Dh	PIE2	—	—	—	—	—	—	—	CCP2IE	---- --0	---- --0
87h	TRISC	PORTC Data Direction Register								1111 1111	1111 1111
11h	TMR2	Timer2 Module's Register								0000 0000	0000 0000
92h	PR2	Timer2 Module's Period Register								1111 1111	1111 1111
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
15h	CCPR1L	Capture/Compare/PWM Register 1 (LSB)								xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Compare/PWM Register 1 (MSB)								xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
1Bh	CCPR2L	Capture/Compare/PWM Register 2 (LSB)								xxxx xxxx	uuuu uuuu
1Ch	CCPR2H	Capture/Compare/PWM Register 2 (MSB)								xxxx xxxx	uuuu uuuu
1Dh	CCP2CON	—	—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	--00 0000

**Legend:** x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by PWM and Timer2.  
**Note 1:** Bits PSPIE and PSPIF are reserved on 28-pin devices; always maintain these bits clear.

**SETUP FOR PWM OPERATION**

The following steps should be taken when configuring the CCP module for PWM operation:

1. Set the PWM period by writing to the PR2 register.
2. Set the PWM duty cycle by writing to the CCPR1L register and CCP1CON<5:4> bits.
3. Make the CCP1 pin an output by clearing the TRISC<2> bit.
4. Set the TMR2 prescale value and enable Timer2 by writing to T2CON.
5. Configure the CCP1 module for PWM operation.



$$\text{PWM Period} = [(PR2) + 1] \cdot 4 \cdot TOSC \cdot (\text{TMR2 Prescale Value})$$

$$\text{PWM Duty Cycle} = (\text{CCPR1L:CCP1CON}<5:4>) \cdot TOSC \cdot (\text{TMR2 Prescale Value})$$

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**T2CON: TIMER2 CONTROL REGISTER (ADDRESS 12h)**

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0
bit 7							bit 0

- bit 7 **Unimplemented:** Read as '0'
- bit 6-3 **TOUTPS3:TOUTPS0:** Timer2 Output Postscale Select bits
  - 0000 = 1:1 postscale
  - 0001 = 1:2 postscale
  - 0010 = 1:3 postscale
  - 
  - 
  - 
  - 1111 = 1:16 postscale
- bit 2 **TMR2ON:** Timer2 On bit
  - 1 = Timer2 is on
  - 0 = Timer2 is off
- bit 1-0 **T2CKPS1:T2CKPS0:** Timer2 Clock Prescale Select bits
  - 00 = Prescaler is 1
  - 01 = Prescaler is 4
  - 1x = Prescaler is 16

<b>Legend:</b>			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown





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**ADCON0 REGISTER (ADDRESS 1Fh)**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	—	ADON
bit 7							bit 0

bit 7-6 **ADCS1:ADCS0**: A/D Conversion Clock Select bits (ADCON0 bits in **bold**)

ADCON1 <ADCS2>	ADCON0 <ADCS1:ADCS0>	Clock Conversion
0	<b>00</b>	Fosc/2
0	<b>01</b>	Fosc/8
0	<b>10</b>	Fosc/32
0	<b>11</b>	Frc (clock derived from the internal A/D RC oscillator)
1	<b>00</b>	Fosc/4
1	<b>01</b>	Fosc/16
1	<b>10</b>	Fosc/64
1	<b>11</b>	Frc (clock derived from the internal A/D RC oscillator)

bit 5-3 **CHS2:CHS0**: Analog Channel Select bits

- 000 = Channel 0 (AN0)
- 001 = Channel 1 (AN1)
- 010 = Channel 2 (AN2)
- 011 = Channel 3 (AN3)
- 100 = Channel 4 (AN4)
- 101 = Channel 5 (AN5)
- 110 = Channel 6 (AN6)
- 111 = Channel 7 (AN7)

**Note:** The PIC16F873A/876A devices only implement A/D channels 0 through 4; the unimplemented selections are reserved. Do not select any unimplemented channels with these devices.

bit 2 **GO/DONE**: A/D Conversion Status bit

When **ADON = 1**:

- 1 = A/D conversion in progress (setting this bit starts the A/D conversion which is automatically cleared by hardware when the A/D conversion is complete)
- 0 = A/D conversion not in progress

bit 1 **Unimplemented**: Read as '0'

bit 0 **ADON**: A/D On bit

- 1 = A/D converter module is powered up
- 0 = A/D converter module is shut-off and consumes no operating current

<b>Legend:</b>			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown



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**ADCON1 REGISTER (ADDRESS 9Fh)**

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	ADCS2	—	—	PCFG3	PCFG2	PCFG1	PCFG0
bit 7				bit 0			

bit 7 **ADFM:** A/D Result Format Select bit

1 = Right justified. Six (6) Most Significant bits of ADRESH are read as '0'.  
 0 = Left justified. Six (6) Least Significant bits of ADRESL are read as '0'.

bit 6 **ADCS2:** A/D Conversion Clock Select bit (ADCON1 bits in shaded area and in bold)

ADCON1 <ADCS2>	ADCON0 <ADCS1:ADCS0>	Clock Conversion
0	00	Fosc/2
0	01	Fosc/8
0	10	Fosc/32
0	11	FRC (clock derived from the internal A/D RC oscillator)
1	00	Fosc/4
1	01	Fosc/16
1	10	Fosc/64
1	11	FRC (clock derived from the internal A/D RC oscillator)

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **PCFG3:PCFG0:** A/D Port Configuration Control bits

PCFG <3:0>	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0	VREF+	VREF-	C/R
0000	A	A	A	A	A	A	A	A	VDD	VSS	8/0
0001	A	A	A	A	VREF+	A	A	A	AN3	VSS	7/1
0010	D	D	D	A	A	A	A	A	VDD	VSS	5/0
0011	D	D	D	A	VREF+	A	A	A	AN3	VSS	4/1
0100	D	D	D	D	A	D	A	A	VDD	VSS	3/0
0101	D	D	D	D	VREF+	D	A	A	AN3	VSS	2/1
011x	D	D	D	D	D	D	D	D	—	—	0/0
1000	A	A	A	A	VREF+	VREF-	A	A	AN3	AN2	6/2
1001	D	D	A	A	A	A	A	A	VDD	VSS	6/0
1010	D	D	A	A	VREF+	A	A	A	AN3	VSS	5/1
1011	D	D	A	A	VREF+	VREF-	A	A	AN3	AN2	4/2
1100	D	D	D	A	VREF+	VREF-	A	A	AN3	AN2	3/2
1101	D	D	D	D	VREF+	VREF-	A	A	AN3	AN2	2/2
1110	D	D	D	D	D	D	D	A	VDD	VSS	1/0
1111	D	D	D	D	VREF+	VREF-	D	A	AN3	AN2	1/2

A = Analog input D = Digital I/O

C/R = # of analog input channels/# of A/D voltage references

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

- n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown





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**REGISTERS/BITS ASSOCIATED WITH A/D**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on MCLR, WDT
0Bh,8Bh,10Bh,18Bh	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF <sup>(1)</sup>	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
8Ch	PIE1	PSPIE <sup>(1)</sup>	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
1Eh	ADRESH	A/D Result Register High Byte								xxxxx xxxxx	uuuu uuuu
9Eh	ADRESL	A/D Result Register Low Byte								xxxxx xxxxx	uuuu uuuu
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	—	ADON	0000 00-0	0000 00-0
9Fh	ADCON1	ADFM	ADCS2	—	—	PCFG3	PCFG2	PCFG1	PCFG0	00-- 0000	00-- 0000
85h	TRISA	—	—	PORTA Data Direction Register						--11 1111	--11 1111
05h	PORTA	—	—	PORTA Data Latch when written: PORTA pins when read						--0x 0000	--0u 0000
89h <sup>(1)</sup>	TRISE	IBF	OBF	IBOV	PSPMODE	—	PORTE Data Direction bits			0000 -111	0000 -111
09h <sup>(1)</sup>	PORTE	—	—	—	—	—	RE2	RE1	RE0	---- -xxxx	---- -uuu

**Legend:** x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used for A/D conversion.

**Note 1:** These registers are not available on 28-pin devices.

**BAUD RATE FORMULA**

SYNC	BRGH = 0 (Low Speed)	BRGH = 1 (High Speed)
0	(Asynchronous) Baud Rate = Fosc/(64 (X + 1))	Baud Rate = Fosc/(16 (X + 1))
1	(Synchronous) Baud Rate = Fosc/(4 (X + 1))	N/A

**Legend:** X = value in SPBRG (0 to 255)

**REGISTERS ASSOCIATED WITH BAUD RATE GENERATOR**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

**Legend:** x = unknown, - = unimplemented, read as '0'. Shaded cells are not used by the BRG.

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**TXSTA: TRANSMIT STATUS AND CONTROL REGISTER (ADDRESS 98h)**

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R-1	R/W-0
CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D

bit 7

bit 0

- bit 7 **CSRC:** Clock Source Select bit  
Asynchronous mode:  
 Don't care.  
Synchronous mode:  
 1 = Master mode (clock generated internally from BRG)  
 0 = Slave mode (clock from external source)
- bit 6 **TX9:** 9-bit Transmit Enable bit  
 1 = Selects 9-bit transmission  
 0 = Selects 8-bit transmission
- bit 5 **TXEN:** Transmit Enable bit  
 1 = Transmit enabled  
 0 = Transmit disabled  
**Note:** SREN/CREN overrides TXEN in Sync mode.
- bit 4 **SYNC:** USART Mode Select bit  
 1 = Synchronous mode  
 0 = Asynchronous mode
- bit 3 **Unimplemented:** Read as '0'
- bit 2 **BRGH:** High Baud Rate Select bit  
Asynchronous mode:  
 1 = High speed  
 0 = Low speed  
Synchronous mode:  
 Unused in this mode.
- bit 1 **TRMT:** Transmit Shift Register Status bit  
 1 = TSR empty  
 0 = TSR full
- bit 0 **TX9D:** 9th bit of Transmit Data, can be Parity bit



<b>Legend:</b>			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

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PROGRAMME : BEJ  
 COURSE CODE : BEC 30403

**RCSTA: RECEIVE STATUS AND CONTROL REGISTER (ADDRESS 18h)**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-x
SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D
bit 7							bit 0

- bit 7     **SPEN:** Serial Port Enable bit  
 1 = Serial port enabled (configures RC7/RX/DT and RC6/TX/CK pins as serial port pins)  
 0 = Serial port disabled
- bit 6     **RX9:** 9-bit Receive Enable bit  
 1 = Selects 9-bit reception  
 0 = Selects 8-bit reception
- bit 5     **SREN:** Single Receive Enable bit  
Asynchronous mode:  
 Don't care.  
Synchronous mode – Master:  
 1 = Enables single receive  
 0 = Disables single receive  
 This bit is cleared after reception is complete.  
Synchronous mode – Slave:  
 Don't care.
- bit 4     **CREN:** Continuous Receive Enable bit  
Asynchronous mode:  
 1 = Enables continuous receive  
 0 = Disables continuous receive  
Synchronous mode:  
 1 = Enables continuous receive until enable bit CREN is cleared (CREN overrides SREN)  
 0 = Disables continuous receive
- bit 3     **ADDEN:** Address Detect Enable bit  
Asynchronous mode 9-bit (RX9 = 1):  
 1 = Enables address detection, enables interrupt and load of the receive buffer when RSR<8>  
 is set  
 0 = Disables address detection, all bytes are received and ninth bit can be used as parity bit
- bit 2     **FERR:** Framing Error bit  
 1 = Framing error (can be updated by reading RCREG register and receive next valid byte)  
 0 = No framing error
- bit 1     **OERR:** Overrun Error bit  
 1 = Overrun error (can be cleared by clearing bit CREN)  
 0 = No overrun error
- bit 0     **RX9D:** 9th bit of Received Data (can be parity bit but must be calculated by user firmware)



<b>Legend:</b>			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown



**FINAL EXAMINATION**

SEMESTER / SESSION : SEM II / 2016/2017  
 COURSE : MICROPROCESSOR AND MICROCONTROLLER

PROGRAMME : BEJ  
 COURSE CODE : BEC 30403

**Instruction Set Summary**

Mnemonic, Operands	Description	Cycles	14-Bit Opcode		Status Affected	Notes
			MSb	LSb		
<b>BYTE-ORIENTED FILE REGISTER OPERATIONS</b>						
ADDWF	f, d	Add W and f	1	00 0111	dfff ffff	C,DC,Z 1,2
ANDWF	f, d	AND W with f	1	00 0101	dfff ffff	Z 1,2
CLRF	f	Clear f	1	00 0001	1fff ffff	Z 2
CLRWF	-	Clear W	1	00 0001	0xxx xxxx	Z
COMF	f, d	Complement f	1	00 1001	dfff ffff	Z 1,2
DECf	f, d	Decrement f	1	00 0011	dfff ffff	Z 1,2
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00 1011	dfff ffff	1,2,3
INCF	f, d	Increment f	1	00 1010	dfff ffff	Z 1,2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00 1111	dfff ffff	1,2,3
IORWF	f, d	Inclusive OR W with f	1	00 0100	dfff ffff	Z 1,2
MOVF	f, d	Move f	1	00 1000	dfff ffff	Z 1,2
MOVWF	f	Move W to f	1	00 0000	1fff ffff	
NOP	-	No Operation	1	00 0000	0xxx 0000	
RLF	f, d	Rotate Left f through Carry	1	00 1101	dfff ffff	C 1,2
RRF	f, d	Rotate Right f through Carry	1	00 1100	dfff ffff	C 1,2
SUBWF	f, d	Subtract W from f	1	00 0010	dfff ffff	C,DC,Z 1,2
SWAPF	f, d	Swap nibbles in f	1	00 1110	dfff ffff	1,2
XORWF	f, d	Exclusive OR W with f	1	00 0110	dfff ffff	Z 1,2
<b>BIT-ORIENTED FILE REGISTER OPERATIONS</b>						
BCF	f, b	Bit Clear f	1	01 00bb	bfff ffff	1,2
BSF	f, b	Bit Set f	1	01 01bb	bfff ffff	1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01 10bb	bfff ffff	3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01 11bb	bfff ffff	3
<b>LITERAL AND CONTROL OPERATIONS</b>						
ADDLW	k	Add Literal and W	1	11 111x	kkkk kkkk	C,DC,Z
ANDLW	k	AND Literal with W	1	11 1001	kkkk kkkk	Z
CALL	k	Call Subroutine	2	10 0k	kkk kkkk kkkk	
CLRWDT	-	Clear Watchdog Timer	1	00 0000	0110 0100	$\overline{TO,PD}$
GOTO	k	Go to Address	2	10 1k	kkk kkkk kkkk	
IORLW	k	Inclusive OR Literal with W	1	11 1000	kkkk kkkk	Z
MOVLW	k	Move Literal to W	1	11 00xx	kkkk kkkk	
RETFIE	-	Return from Interrupt	2	00 0000	0000 1001	
RETLW	k	Return with Literal in W	2	11 01xx	kkkk kkkk	
RETURN	-	Return from Subroutine	2	00 0000	0000 1000	
SLEEP	-	Go into Standby mode	1	00 0000	0110 0011	$\overline{TO,PD}$
SUBLW	k	Subtract W from Literal	1	11 110x	kkkk kkkk	C,DC,Z
XORLW	k	Exclusive OR Literal with W	1	11 1010	kkkk kkkk	Z



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