Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2016/2017

COURSE NAME	:	COMPUTER ARCHITECTURE AND ORGANIZATION
COURSE CODE	:	BEC30303
PROGRAMME CODE	:	BEJ
EXAMINATION DATE	:	JUNE 2017
DURATION	:	3 HOURS
INSTRUCTION	:	ANSWER **ALL** QUESTIONS

THIS QUESTION PAPER CONSISTS OF EIGHT **(8)** PAGES

SECTION A (OBJECTIVE QUESTIONS)

Q1 The ALU makes use of _____ to store the intermediate results.

a) accumulators
b) calculators
c) registers
d) stack

(1 mark)

Q2 The control unit controls other units by generating ____.

a) control signals
b) timing signals
c) traffic signals
d) transfer signals

(1 mark)

Q3 A CPU generally handles interrupt by executing an interrupt service routine _____.

a) as soon as an interrupt is raised
b) by checking the interrupt register at the end of fetch cycle
c) by checking the interrupt register after finishing the execution of the current instruction
d) by checking the interrupt register at fixed time intervals

(1 mark)

Q4 An interface that provides I/O transfer of data directly to and from the memory unit and peripheral is termed as _____.

a) DDA
b) serial interface
c) BR (Bus Request)
d) DMA

(1 mark)

Q5 Suppose a processor does not have any stack pointer register. Which of the following statements is true?

a) It cannot have subroutine call instruction.
b) It can have subroutine call instruction, but no nested subroutine calls.
c) Nested subroutine calls are possible, but interrupts are not.
d) All sequences of subroutine calls and also interrupts are possible.

(1 mark)

Q6 The main advantage of multiple bus organization over single bus is _____.
a) reduction in the number of cycles for execution.
b) increase in size of the registers
c) better connectivity
d) none of these

(1 mark)

Q7 Data transfer between the main memory and the CPU register takes place through two registers namely _____ .
a) MAR and MDR
b) MAR and Accumulator
c) accumulator and program counter
d) general purpose register and MDR

(1 mark)

Q8 In a vectored interrupt, _____.
a) the branch address is assigned to a fixed location in memory
b) the branch address is obtained from a register in the processor
c) the interrupting source supplies the branch information to the processor through an interrupt vector
d) none of the above

(1 mark)

Q9 A memory management technique used to improve computer performance is _____.
a) storing as much data as possible on disk
b) selecting memory chips based on their cost
c) using the cache to store data that will most likely be needed soon
d) preventing data from being moved from the cache to primary memory

(1 mark)

Q10 The performance of a pipelined processor suffers if _____.
a) the pipelined stages have different delays
b) the pipeline stages share hardware resources
c) consecutive instructions are dependent on each other
d) all the above

(1 mark)

Q11 Interrupts can be generated in response to _____.

i. detected program errors such as arithmetic overflow or division by zero
ii. detected hardware faults
iii. input/output activities
iv. internal timers

a) i, ii, and iii
b) i, ii, and iv
c) i, iii, and iv
d) ii, iii, and iv
e) i, ii, iii, and iv

(2 marks)

Q12 In Reverse Polish notation, expression A*B+C*D is written as _____.

a) AB*CD*+
b) A*BCD*+
c) AB*CD+*
d) A*B*CD+

(2 marks)

Q13 Two processors A and B have clock frequencies of 700 MHz and 900 MHz respectively. Suppose A can execute an instruction with an average of 3 steps and B can execute with an average of 5 steps. For the execution of the same instruction which processor is faster?

a) A
b) B
c) Both takes the same time
d) Insuffient information

(2 marks)

Q14 When we use auto increment or auto decrement, which of the following is/are true

i. In both, the address is used to retrieve the operand and then the address gets altered.
ii. In auto increment the operand is retrieved first and then the address altered.
iii. Both of them can be used on general purpose registers as well as memory locations.

a) ii
b) i and ii
c) i and iii
d) ii and iii
e) i, ii, and iii

(2 marks)

Q15 How many 32K X 1 RAM chips are needed to provide a memory capacity of 256kB?

a) 8
b) 32
c) 64
d) 128
e) 256

(2 marks)

Q16 Which is the most appropriate match for the items in the first column with the items in the second column

(X.) Indirect Addressing	(I.) Array implementation
(Y.) Indexed Addressing	(II.) Writing re-locatable code
(Z.) Base Register Addressing	(III.) Passing array as parameter

a) (X, III) (Y, I) (Z, II).
b) (X, II) (Y, III) (Z, I).
c) (X, III) (Y, II) (Z, I).
d) (X, I) (Y, III) (Z, II).
e) (X, I) (Y, II) (Z, III).

(2 marks)

Q17 The instruction *add R0, R1* has the register transfer interpretation *R0 <= R0 + R1*. The minimum number of clock cycles needed for execution cycle of this instruction is _____.

a) 2
b) 3
c) 4
d) 5

(2 marks)

Q18 A computer's memory is composed of 4K words of 32 bits each. How many total bits in memory?

a) 12800
b) 1280000
c) 1310720
d) 131072

(2 marks)

Q19 The maximum addressing capacity of a microprocessor which uses 16 bit database and 32 bit address base is _____.

a) 32
b) 64
c) 4 GB
d) both (A) & (B)
e) none of the above

(2 marks)

Q20 A computer's memory is composed of 8K words of 32 bits each, and a byte is 8 bits. How many bytes does this memory contain?

a) 8K
b) 32K
c) 16K
d) 4K
e) 64K

(2 marks)

SECTION B (SUBJECTIVE QUESTIONS)

Q21 (a) Basically, computer organization have five (5) basic functional units of a general-purpose computer. Explain briefly each of them.

(5 marks)

(b) Calculate the total execution time for CPU 1 to run the C program as shown in **Table Q21(b)**.

Table Q21(b)

Micro-processor	Instruction characteristics	Microprocessor speed
CPU 1	Total 150 instructions (20 instructions need 3 cycles per instruction, 65 instructions need 2 cycles per instruction, 65 instructions need 1 cycle per instruction)	2.4 GHz

(5 marks)

Q22 (a) Write the code to perform the computation X = (B + A) * [D * (E – C) + G] using microprocessors that use the following instruction formats based on CISC type.

(i) Three-address instruction

(5 marks)

(ii) Two-address instruction

(8 marks)

(b) Convert the following expressions from Postfix to Infix notation.

(i) 223*5+*

(2 marks)

(ii) 34+2034*2+-*

(2 marks)

(iii) 534+*22212+*+*-

(3 marks)

Q23 (a) Identify the differences between hardwired and micro-programmed control unit for the following attributes:

(i) speed
(ii) cost of implementation
(iii) flexibility
(iv) ability to handle complex instructions
(v) instruction set size

(5 marks)

(b) On a synchronous bus, all devices derive timing information from a control line called the bus clock. Elaborate the processes involved by using an appropriate diagram to support your answer.

(5 marks)

Q24 (a) List two (2) types of electronic gadgets using USB protocol for their communication.

(2 marks)

(b) Give reasons for electronic gadgets in adopting USB protocol?

(2 marks)

(c) Differentiate between interrupt-driven I/O, isolated I/O, and memory-mapped I/O.

(6 marks)

Q25 Several instructions will be executed by UTHM™ processor having 4-stage pipelined architecture. The instruction cycle comprises 4 steps; *fetch (F), decode (D), execute (E), and write back (W)*, where all steps require 1 clock cycle except the execute step, which takes 3 clock cycles. Assume 1 *clock cycle* = 10 *ns*.

(a) Sketch the space time diagram to execute four (4) instructions.

(6 marks)

(b) Calculate the total execution time (in *ns*) needed by the pipelined computer to execute a C++ program having 1500 instructions.

(2 marks)

(c) Calculate the performance speed up of the pipelined computer over non-pipelined computer to execute similar C++ program in **Q25(b)**.

(2 marks)

Q26 (a) Differentiate the memory access time between primary storage and secondary storage.

(4 marks)

(b) Referring to **Figure Q26(b),** describe the function of element X.

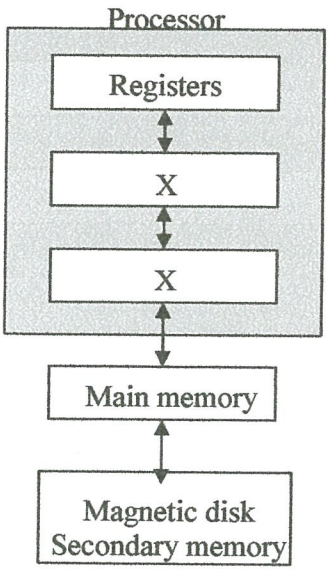

Figure Q26(b)

(4 marks)

(c) From **Table Q26(c),** determine the miss penalty in *ns* when a L2 cache miss occurs. Assume 1 clock cycle = 5 ns.

Table Q26(c)

Memory Level	Processor Clock Cycle (*ns*)
L1 cache	2
L2 cache	5
L3 cache	8
DDR4 RAM	60
Hard disk	100

(2 marks)

- **END OF QUESTIONS –**