UTHM
Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER 2
SESSION 2016/2017

COURSE NAME	:	ANALOG ELECTRONICS
COURSE CODE	:	BEL 10203
PROGRAMME	:	BEJ / BEV
TEST DATE	:	JUNE 2017
DURATION	:	3 HOURS
INSTRUCTION	:	ANSWER **ALL** QUESTIONS.

THIS QUESTION PAPER CONSISTS OF **SEVEN (7)** PAGES

Q1 (a) A P-N (positive-negative) junction is a boundary or interface between two types of semiconductor material, p-type and n-type, inside a single crystal of semiconductor. In your own words and with the aid of diagram,

(i) discuss the formation of depletion region in a P-N junction

(4 marks)

(ii) explain the effect if forward biased voltage is applied across a silicon P-N diode.

(3 marks)

(b) **Figure Q1 (b)** showed an example of a clipper circuit designed to prevent the output of a circuit from exceeding a predetermined voltage level. Given that the input voltage, V_i, is a triangular wave with $V_{p\text{-}p} = 20$ V.

(i) With the aid of diagrams, determine the output of this circuit assuming that D_1 and D_2 are silicon diode.

(5 marks)

(ii) Label your input and output waveform accordingly.

(4 marks)

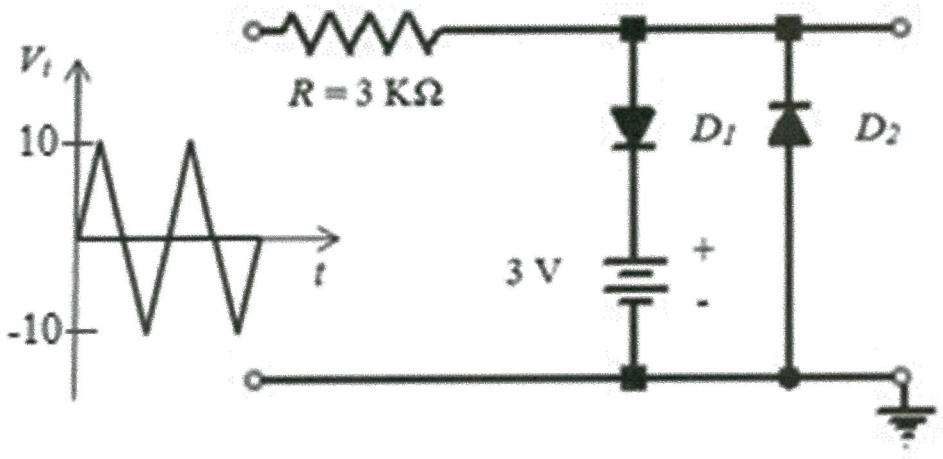

Figure Q1 (b)

(c) Based on the zener diode circuit shown in **Figure Q1 (c)**, the knee current, I_K, of this ideal zener diode is given by 10 mA. Using the information provided in this diagram, and with the voltage drop maintained at 5 volts across the load, R_L,

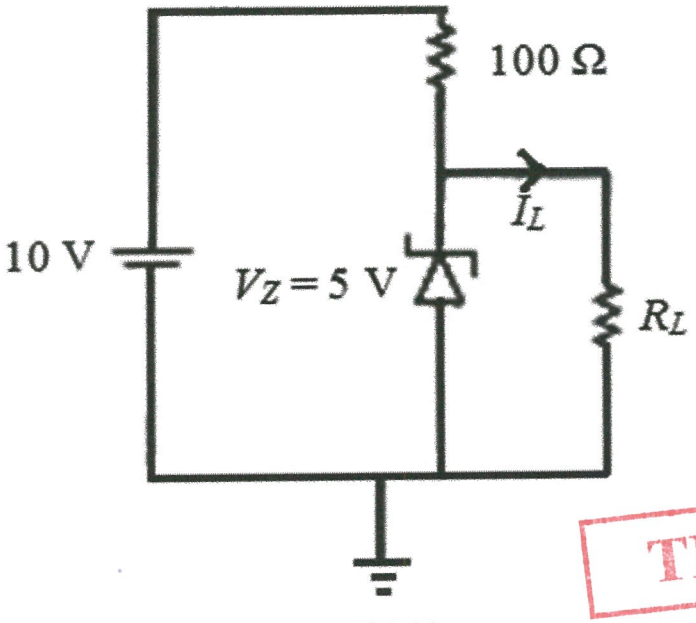

Figure Q1 (c)

(i) Determine the minimum resistance value of load, R_L.

(5 marks)

(ii) Calculate the minimum power rating of the zener diode.

(4 marks)

Q2 (a) With the help of an output characteristic diagram (I_C versus V_{CE}), explain how to determine the DC Load Line in fixed biased BJT circuit.

(3 marks)

(b) In **Figure Q2 (b)**, another 9.1 kΩ resistor is added at the base terminal to the ground. Other specifications for this biasing circuit are: R_C = 3.9 kΩ, R_E = 0.68 kΩ, R = 62 kΩ, Vcc =16 V and β = 80.

(i) Draw the new circuit and state the name of the circuit.

(2 marks)

(ii) Determine suitable method to analyse this circuit.

(2 marks)

(iii) Estimate I_B and I_E currents.

(5 marks)

(iv) Determine V_{CE} voltage.

(2 marks)

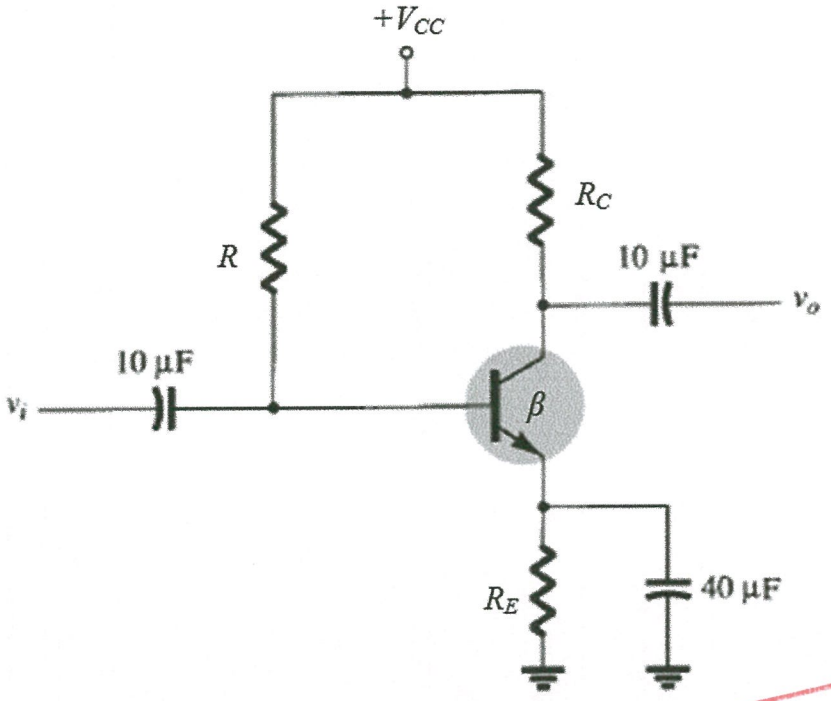

Figure Q2 (b)

(c) Based on the new circuit that you have drawn in **Q2 (b) (i)** above, if r_o is 50 kΩ, determine following parameters:

(i) Draw the *re* model AC equivalent circuit.

(3 marks)

(ii) Find *re* value.

(1 mark)

(iii) Determine Z_i and Z_o.

(5 marks)

(iv) Calculate A_v.

(2 marks)

Q3 (a) Briefly discuss the significant differences between a p-channel JFET and p-channel E-MOSFET in terms of the construction and operation.

(6 marks)

(b) Design a self-bias amplifier circuit using a JFET transistor with I_{DSS} = 8 mA and V_P = -6 V to have a Q-point at I_{DQ} = 4 mA using a supply of 14V. Assume that $R_D = 3R_S$.

(10 marks)

(c) The major advantage of FETs is their very high input resistance, which makes them very useful in amplifier circuit. Based on the amplifier circuit with common-source voltage divider configuration shown in **Figure Q3(c)**,

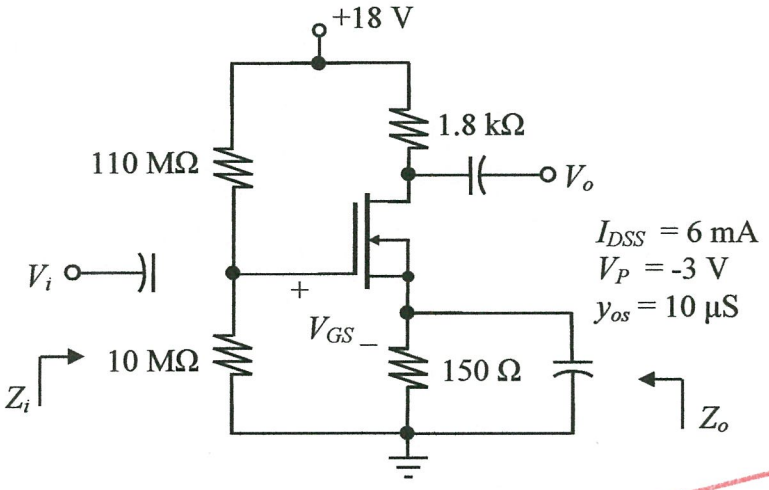

Figure Q3 (c)

(i) sketch the ac equivalent circuit

(2 marks)

(ii) determine the Z_i, Z_o and A_v if the resulting V_{GSQ} = +0.35V and I_{DQ} = 7.6mA

(7 marks)

Q4 (a) **Figure Q4 (a)** shows a BJT amplifier. At low frequency response, Coupling capacitors (C_s, C_c) and Bypass capacitor (C_E) will have capacitive reactance X_c that will affect the circuit impedance.

(i) Derive the cutoff frequency (f_{LS}, f_{LC}, f_{LE}) due to each capacitor (C_s, C_c, C_E).

(6 marks)

(ii) Draw the resultant bode plot for this circuit.

(4 marks)

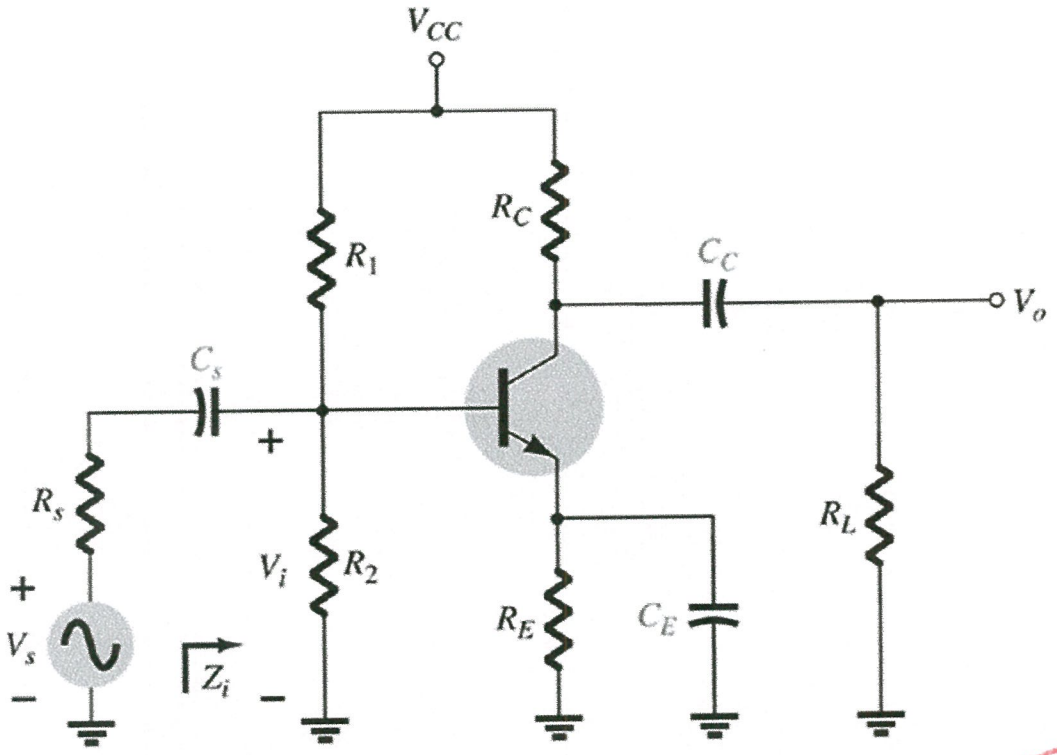

Figure Q4 (a)

(b) Explain the Miller Effect Capacitance.

(3 marks)

(c) **Figure Q4 (c)** shows a biased-class B amplifier:

(i) Explain with the aid of a diagram how cross-over distortion problem occur for class B amplifier.

(6 marks)

(ii) Determine the value of resistor R_2 to provide trickle current for distortion free output. Given R_1 =300 Ω, R_L= 16 Ω and V_{cc} = 30V. V_{BE} for each transistor is 0.7 V.

(6 marks)

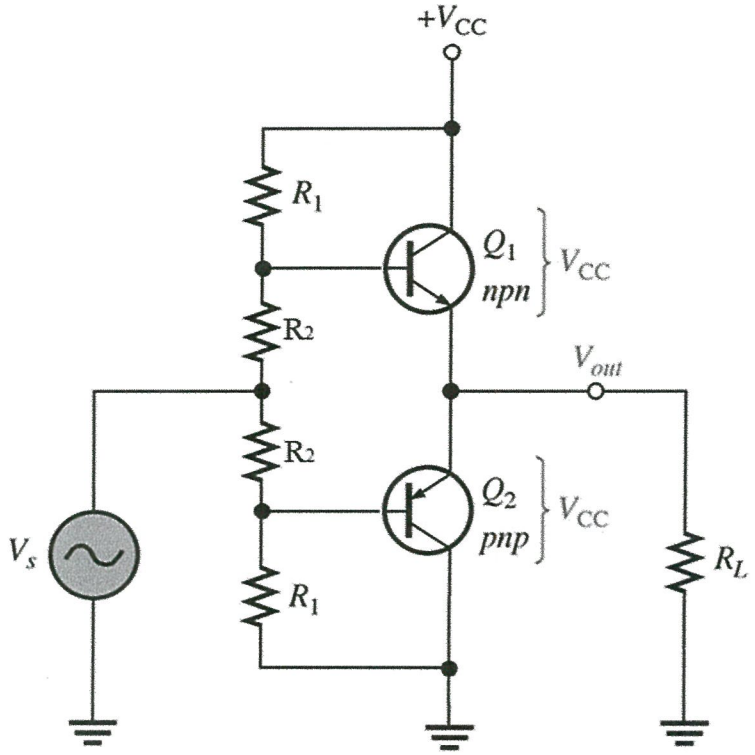

Figure Q4 (c)

- END OF QUESTION -