Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2016/2017

COURSE NAME	: ADVANCED MICROCONTROLLER
COURSE CODE	: BEC 41103
PROGRAMME	: BEJ
EXAMINATION DATE	: JUNE 2017
DURATION	: 3 HOURS
INSTRUCTION	: ANSWER **ALL** QUESTIONS

THIS QUESTION PAPER CONSISTS OF **SIXTEEN (16)** PAGES.

Q1 (a) With visual aid, briefly describe standard features of PIC microcontroller.

(8 marks)

(b) Distinguish the difference between two components of data RAM or data memory space.

(3 marks)

(c) Answer the following questions based on the program given in **Figure Q1(c)**.

```
#include <P18F4520.h>
#pragma idata x = 0x104
unsigned char x = 5;
#pragma idata y = 0x105
unsigned char y = 9;
#pragma udata z = 0x106
unsigned char z;
void main(void)
  {
     TRISB = 0;
     z = x + y;
     PORTB = z;
  }
```

Figure Q1(c)

(i) Describe the role of #pragma directive in **Figure Q1(c)**.

(2 marks)

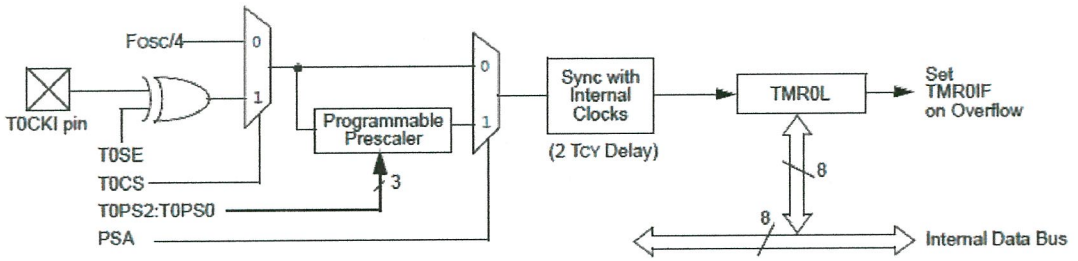
(ii) Identify the memory space that utilized to store the data in **Figure Q1(c)**. Justify your answer.

(3 marks)

(iii) Examine the contents in addresses 0x104, 0x105 and 0x106 after excuting the program in **Figure Q1(c)**.

(4 marks)

Q2 **Figure Q2** shows Timer0 block diagram. Answer the following questions based on **Figure Q2**.



Note: Upon Reset, Timer0 is enabled in 8-bit mode with clock input from T0CKI max. prescale.

Figure Q2

(a) Analyze the block diagram in **Figure Q2** to identify the minimum and maximum values to be loaded into TMR0L when the Timer0 is employed to generate delay. Justify your answer.

(3 marks)

(b) Explain the purpose of programmable prescaler in Timer0.

(2 marks)

(c) What is the highest size of prescaler supported by Timer0.

(1 mark)

(d) If internal clock frequency is 20MHz. Calculate the longest delay time that could be generated by using the Timer0.

(2 marks)

(e) Write a delay function in C to generate the longest delay as calculated in Q2(d) using the timer in **Figure Q2**. Assume clock frequency is 20MHz.

(i) Create a flow chart for the delay function.

(5 marks)

(ii) Compute delay function using C program.

(7 marks)

Q3 **Figure Q3** shows EUSART transmit block diagram of PIC18 microcontroller that could be configured for serial data transfer.

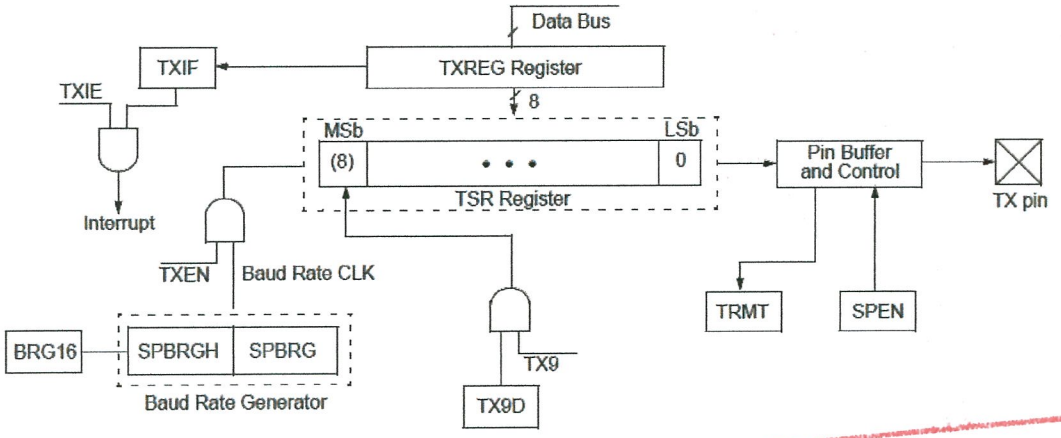


Figure Q3

(a) Explain the role of the TXREG register in serial data transfer.

(2 marks)

(b) If the circuit in **Figure Q3** is utilized for transmitting the ASCII character "E" (0100 0101 in binary) with no parity bit and one stop bit. Create the sequence of bits that framed to transfer serially via TX pin.

(6 marks)

(c) Determine the value to be loaded in the SPBRG register, if **Figure Q3** is configured to transfer a character "E" in serial. Considering crystal frequency is 10MHz, BRGH bit is cleared and transfer rate is 9600 baud.

(4 marks)

(d) Determine the byte to be loaded in the TXSTA register.

(2 marks)

(e) Write a C program to transmit the character "E" via TX pin.

(6 marks)

Q4 (a) Interrupt and polling are two methods to provide services to devices. Explain which technique avoids tying down the microcontroller. Justify your answer.

(3 marks)

(b) Discuss the steps microcontroller handles an interrupt.

(5 marks)

(c) **Figure Q4(c)** shows INT0-INT2 interrupts.

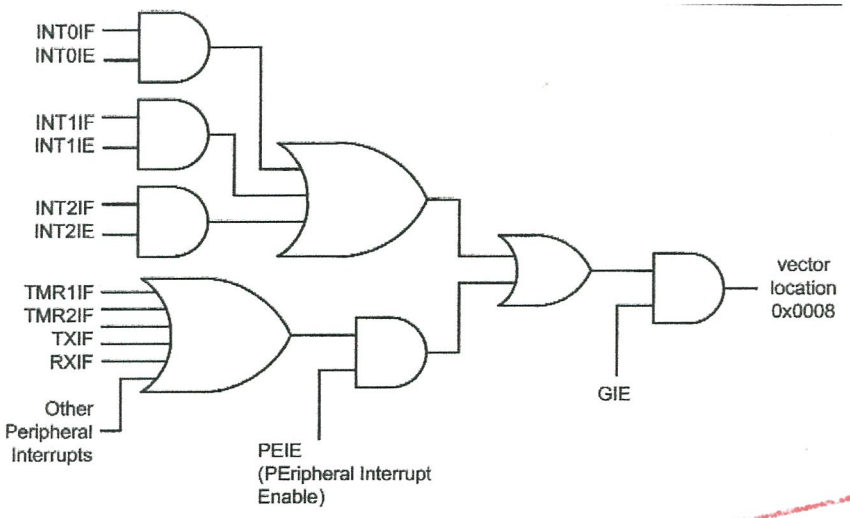


Figure Q4(c)

(i) Write a single instruction to disable all INT0-INT2 interrupts.

(2 marks)

(ii) Write instructions to configure INT1 as high priority external hardware interrupt that activates at positive edge-triggered.

(10 marks)

Q5 (a) Analyze the program in **Figure Q5** and answer the following questions.

(i) Identify the main purpose of the program.

(4 marks)

(ii) Describe the role of TBLPTR in the program.

(2 marks)

(iii) Determine the data to be written to in the program.

(2 marks)

(iv) Examine instructions in Part II of the program **Figure Q5**. Summarize the outcome after executing the instructions in Part II.

(4 marks)

(b) Networking system is needed to provide connection between different devices. Suggest a suitable network connection between keyboard, mouse PCs and printers without physical cables and the signal from device can through penetrate walls. Justify the reason of your suggestion.

(4 marks)

(c) WiFi and Bluetooth are two approaches to establish wireless network. Compare between WiFi dan Bluetooth and discuss **TWO (2)** differences between them.

(4 marks)

```
//Program Figure Q5

#include <p18f4520.h>
void Delay(unsigned int itime);

void main ( )
{
    unsigned char x;

    //Part I
    TBLPTR = (short long) 0x0400;
    TABLAT = 'G';
    _asm TBLWTPOSTINC _endasm
    TABLAT = 'O';
    _asm TBLWTPOSTINC _endasm
    TABLAT = 'O';
```

```
_asm TBLWTPOSTINC _endasm
TABLAT = 'D';
_asm TBLWTPOSTINC _endasm
TABLAT = ' ';
_asm TBLWTPOSTINC _endasm
TABLAT = 'B';
_asm TBLWTPOSTINC _endasm
TABLAT = 'Y';
_asm TBLWTPOSTINC _endasm
TABLAT = 'E';
_asm TBLWTPOSTINC _endasm

//Part II
TBLPTR = (short long)0x0400;
EECON1bits.EEPGD = 1;
EECON1bits.CFGS = 0;
EECON1bits.WREN = 1;
INTCONbits.GIE = 0;
EECON2 = 0x55;
EECON2 = 0xAA;
EECON1bits.WR=1;
_asm NOP _endasm
INTCONbits.GIE = 1;
EECON1bits.WREN = 0;

//Part III
TALPTR = (short long) 0x0400;
for(x=0;x<8;x++)
  {
   _asm TBLRDPOSTINC _endasm
   PORTB = TABLAT;
   Delay(250);
   }
}
```

Figure Q5

- **End of Questions** -

FINAL EXAMINATION

SEMESTER / SESSION : SEM II / 2016/2017 PROGRAMME : BEJ
COURSE : ADVANCED MICROCONTROLLER COURSE CODE : BEC 41103

T0CON: Timer0 Control Register

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
TMR0ON	T08BIT	T0CS	T0SE	PSA	T0PS2	T0PS1	T0PS0
bit 7							bit 0

TMR0ON: Timer0 On/Off Control bit
1 = Enables Timer0
0 = Stops Timer0

T08BIT: Timer0 8-bit/16-bit Control bit
1 = Timer0 is configured as an 8-bit timer/counter
0 = Timer0 is configured as a 16-bit timer/counter

T0CS: Timer0 Clock Source Select bit
1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (CLKO)

T0SE: Timer0 Source Edge Select bit
1 = Increment on high-to-low transition on T0CKI pin
0 = Increment on low-to-high transition on T0CKI pin

PSA: Timer0 Prescaler Assignment bit
1 = TImer0 prescaler is NOT assigned. Timer0 clock input bypasses prescaler.
0 = Timer0 prescaler is assigned. Timer0 clock input comes from prescaler output.

T0PS2:T0PS0: Timer0 Prescaler Select bits
111 = 1:256 prescale value
110 = 1:128 prescale value
101 = 1:64 prescale value
100 = 1:32 prescale value
011 = 1:16 prescale value
010 = 1:8 prescale value
001 = 1:4 prescale value
000 = 1:2 prescale value

FINAL EXAMINATION

SEMESTER / SESSION : SEM II / 2016/2017 PROGRAMME : BEJ
COURSE : ADVANCED MICROCONTROLLER COURSE CODE : BEC 41103

TXSTA (Transmit Status and Control Register)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-1	R/W-0
CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D
bit 7							bit 0

CSRC: Clock Source Select bit

Asynchronous mode:
Don't care.

Synchronous mode:
1 = Master mode (clock generated internally from BRG)
0 = Slave mode (clock from external source)

TX9: 9-bit Transmit Enable bit

1 = Selects 9-bit transmission
0 = Selects 8-bit transmission

TXEN: Transmit Enable bit

1 = Transmit enabled
0 = Transmit disabled

Note: SREN/CREN overrides TXEN in Sync mode.

SYNC: EUSART Mode Select bit

1 = Synchronous mode
0 = Asynchronous mode

SENDB: Send Break Character bit

Asynchronous mode:
1 = Send Sync Break on next transmission (cleared by hardware upon completion)
0 = Sync Break transmission completed

Synchronous mode:
Don't care.

BRGH: High Baud Rate Select bit

Asynchronous mode:
1 = High speed
0 = Low speed

Synchronous mode:
Unused in this mode.

TRMT: Transmit Shift Register Status bit

1 = TSR empty
0 = TSR full

TX9D: 9th bit of Transmit Data

Can be address/data bit or a parity bit.

FINAL EXAMINATION

SEMESTER / SESSION : SEM II / 2016/2017 PROGRAMME : BEJ
COURSE : ADVANCED MICROCONTROLLER COURSE CODE : BEC 41103

RCSTA (Receive Status and Control Register)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-x
SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D
bit 7							bit 0

SPEN: Serial Port Enable bit
1 = Serial port enabled (configures RX/DT and TX/CK pins as serial port pins)
0 = Serial port disabled (held in Reset)

RX9: 9-bit Receive Enable bit
1 = Selects 9-bit reception
0 = Selects 8-bit reception

SREN: Single Receive Enable bit
Asynchronous mode:
Don't care.
Synchronous mode – Master:
1 = Enables single receive
0 = Disables single receive
This bit is cleared after reception is complete.
Synchronous mode – Slave:
Don't care.

CREN: Continuous Receive Enable bit
Asynchronous mode:
1 = Enables receiver
0 = Disables receiver
Synchronous mode:
1 = Enables continuous receive until enable bit CREN is cleared (CREN overrides SREN)
0 = Disables continuous receive

ADDEN: Address Detect Enable bit
Asynchronous mode 9-bit (RX9 = 1):
1 = Enables address detection, enables interrupt and loads the receive buffer when RSR<8> is set
0 = Disables address detection, all bytes are received and ninth bit can be used as parity bit
Asynchronous mode 9-bit (RX9 = 0):
Don't care.

FERR: Framing Error bit
1 = Framing error (can be updated by reading RCREG register and receiving next valid byte)
0 = No framing error

OERR: Overrun Error bit
1 = Overrun error (can be cleared by clearing bit CREN)
0 = No overrun error

RX9D: 9th bit of Received Data
This can be address/data bit or a parity bit and must be calculated by user firmware.

FINAL EXAMINATION

SEMESTER / SESSION : SEM II / 2016/2017 PROGRAMME : BEJ
COURSE : ADVANCED MICROCONTROLLER COURSE CODE : BEC 41103

PIR1 (Peripheral Interrupt Request (Flag) Register 1

R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
PSPIF(1)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF
bit 7							bit 0

PSPIF: Parallel Slave Port Read/Write Interrupt Flag bit(1)
1 = A read or a write operation has taken place (must be cleared in software)
0 = No read or write has occurred

Note 1: This bit is unimplemented on 28-pin devices and will read as '0'.

ADIF: A/D Converter Interrupt Flag bit
1 = An A/D conversion completed (must be cleared in software)
0 = The A/D conversion is not complete

RCIF: EUSART Receive Interrupt Flag bit
1 = The EUSART receive buffer, RCREG, is full (cleared when RCREG is read)
0 = The EUSART receive buffer is empty

TXIF: EUSART Transmit Interrupt Flag bit
1 = The EUSART transmit buffer, TXREG, is empty (cleared when TXREG is written)
0 = The EUSART transmit buffer is full

SSPIF: Master Synchronous Serial Port Interrupt Flag bit
1 = The transmission/reception is complete (must be cleared in software)
0 = Waiting to transmit/receive

CCP1IF: CCP1 Interrupt Flag bit

Capture mode:
1 = A TMR1 register capture occurred (must be cleared in software)
0 = No TMR1 register capture occurred

Compare mode:
1 = A TMR1 register compare match occurred (must be cleared in software)
0 = No TMR1 register compare match occurred

PWM mode:
Unused in this mode.

TMR2IF: TMR2 to PR2 Match Interrupt Flag bit
1 = TMR2 to PR2 match occurred (must be cleared in software)
0 = No TMR2 to PR2 match occurred

TMR1IF: TMR1 Overflow Interrupt Flag bit
1 = TMR1 register overflowed (must be cleared in software)
0 = TMR1 register did not overflow

FINAL EXAMINATION

SEMESTER / SESSION : SEM II / 2016/2017
COURSE : ADVANCED MICROCONTROLLER
PROGRAMME : BEJ
COURSE CODE : BEC 41103

EECON1 (EEPROM Control Register)

R/W-x	R/W-x	U-0	R/W-0	R/W-x	R/W-0	R/S-0	R/S-0
EEPGD	CFGS	—	FREE	WRERR	WREN	WR	RD

bit 7 bit 0

EEPGD: Flash Program or Data EEPROM Memory Select bit
1 = Access Flash program memory
0 = Access data EEPROM memory

CFGS: Flash Program/Data EEPROM or Configuration Select bit
1 = Access Configuration registers
0 = Access Flash program or data EEPROM memory

Unimplemented: Read as '0'

FREE: Flash Row Erase Enable bit
1 = Erase the program memory row addressed by TBLPTR on the next WR command (cleared by completion of erase operation)
0 = Perform write only

WRERR: Flash Program/Data EEPROM Error Flag bit
1 = A write operation is prematurely terminated (any Reset during self-timed programming in normal operation, or an improper write attempt)
0 = The write operation completed

Note: When a WRERR occurs, the EEPGD and CFGS bits are not cleared. This allows tracing of the error condition.

WREN: Flash Program/Data EEPROM Write Enable bit
1 = Allows write cycles to Flash program/data EEPROM
0 = Inhibits write cycles to Flash program/data EEPROM

WR: Write Control bit
1 = Initiates a data EEPROM erase/write cycle or a program memory erase cycle or write cycle. (The operation is self-timed and the bit is cleared by hardware once write is complete. The WR bit can only be set (not cleared) in software.)
0 = Write cycle to the EEPROM is complete

RD: Read Control bit
1 = Initiates an EEPROM read (Read takes one cycle. RD is cleared in hardware. The RD bit can only be set (not cleared) in software. RD bit cannot be set when EEPGD = 1 or CFGS = 1.)
0 = Does not initiate an EEPROM read

FINAL EXAMINATION

SEMESTER / SESSION : SEM II / 2016/2017 PROGRAMME : BEJ
COURSE : ADVANCED MICROCONTROLLER COURSE CODE : BEC 41103

INTCON Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF
bit 7							bit 0

GIE/GIEH: Global Interrupt Enable bit

When IPEN = 0:
1 = Enables all unmasked interrupts
0 = Disables all interrupts

When IPEN = 1:
1 = Enables all high priority interrupts
0 = Disables all interrupts

PEIE/GIEL: Peripheral Interrupt Enable bit

When IPEN = 0:
1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts

When IPEN = 1:
1 = Enables all low priority peripheral interrupts
0 = Disables all low priority peripheral interrupts

TMR0IE: TMR0 Overflow Interrupt Enable bit

1 = Enables the TMR0 overflow interrupt
0 = Disables the TMR0 overflow interrupt

INT0IE: INT0 External Interrupt Enable bit

1 = Enables the INT0 external interrupt
0 = Disables the INT0 external interrupt

RBIE: RB Port Change Interrupt Enable bit

1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

TMR0IF: TMR0 Overflow Interrupt Flag bit

1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

INT0IF: INT0 External Interrupt Flag bit

1 = The INT0 external interrupt occurred (must be cleared in software)
0 = The INT0 external interrupt did not occur

RBIF: RB Port Change Interrupt Flag bit

1 = At least one of the RB7:RB4 pins changed state (must be cleared in software)
0 = None of the RB7:RB4 pins have changed state

Note: A mismatch condition will continue to set this bit. Reading PORTB will end the mismatch condition and allow the bit to be cleared.

FINAL EXAMINATION

SEMESTER / SESSION : SEM II / 2016/2017 PROGRAMME : BEJ
COURSE : ADVANCED MICROCONTROLLER COURSE CODE : BEC 41103

INTCON2 Register

R/W-1	R/W-1	R/W-1	R/W-1	U-0	R/W-1	U-0	R/W-1
$\overline{\text{RBPU}}$	INTEDG0	INTEDG1	INTEDG2	—	TMR0IP	—	RBIP
bit 7							bit 0

$\overline{\text{RBPU}}$: PORTB Pull-up Enable bit
1 = All PORTB pull-ups are disabled
0 = PORTB pull-ups are enabled by individual port latch values

INTEDG0: External Interrupt 0 Edge Select bit
1 = Interrupt on rising edge
0 = Interrupt on falling edge

INTEDG1: External Interrupt 1 Edge Select bit
1 = Interrupt on rising edge
0 = Interrupt on falling edge

INTEDG2: External Interrupt 2 Edge Select bit
1 = Interrupt on rising edge
0 = Interrupt on falling edge

Unimplemented: Read as '0'

TMR0IP: TMR0 Overflow Interrupt Priority bit
1 = High priority
0 = Low priority

Unimplemented: Read as '0'

RBIP: RB Port Change Interrupt Priority bit
1 = High priority
0 = Low priority

FINAL EXAMINATION

SEMESTER / SESSION : SEM II / 2016/2017 PROGRAMME : BEJ
COURSE : ADVANCED MICROCONTROLLER COURSE CODE : BEC 41103

INTCON3 Register

R/W-1	R/W-1	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
INT2IP	INT1IP	—	INT2IE	INT1IE	—	INT2IF	INT1IF
bit 7							bit 0

INT2IP: INT2 External Interrupt Priority bit
1 = High priority
0 = Low priority

INT1IP: INT1 External Interrupt Priority bit
1 = High priority
0 = Low priority

Unimplemented: Read as '0'

INT2IE: INT2 External Interrupt Enable bit
1 = Enables the INT2 external interrupt
0 = Disables the INT2 external interrupt

INT1IE: INT1 External Interrupt Enable bit
1 = Enables the INT1 external interrupt
0 = Disables the INT1 external interrupt

Unimplemented: Read as '0'

INT2IF: INT2 External Interrupt Flag bit
1 = The INT2 external interrupt occurred (must be cleared in software)
0 = The INT2 external interrupt did not occur

INT1IF: INT1 External Interrupt Flag bit
1 = The INT1 external interrupt occurred (must be cleared in software)
0 = The INT1 external interrupt did not occur

FINAL EXAMINATION

SEMESTER / SESSION : SEM II / 2016/2017 PROGRAMME : BEJ
COURSE : ADVANCED MICROCONTROLLER COURSE CODE : BEC 41103

RCON Register

R/W-0	R/W-1(1)	U-0	R/W-1	R-1	R-1	R/W-0(1)	R/W-0
IPEN	SBOREN	—	$\overline{RI}$	$\overline{TO}$	$\overline{PD}$	$\overline{POR}$	$\overline{BOR}$
bit 7							bit 0

IPEN: Interrupt Priority Enable bit
1 = Enable priority levels on interrupts
0 = Disable priority levels on interrupts (PIC16XXX Compatibility mode)
SBOREN: Software BOR Enable bit(1)
For details of bit operation, see Register 4-1.

Note 1: Actual Reset values are determined by device configuration and the nature of the device Reset. See Register 4-1 for additional information.

Unimplemented: Read as '0'
$\overline{RI}$: RESET Instruction Flag bit
For details of bit operation, see Register 4-1.
$\overline{TO}$: Watchdog Time-out Flag bit
For details of bit operation, see Register 4-1.
$\overline{PD}$: Power-down Detection Flag bit
For details of bit operation, see Register 4-1.
$\overline{POR}$: Power-on Reset Status bit
For details of bit operation, see Register 4-1.
$\overline{BOR}$: Brown-out Reset Status bit
For details of bit operation, see Register 4-1.