Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2016/2017

COURSE NAME	:	COMPUTER ARCHITECTURE AND ORGANIZATION
COURSE CODE	:	BEC 30303
PROGRAMME CODE	:	BEJ
EXAMINATION DATE	:	DECEMBER 2016 / JANUARY 2017
DURATION	:	3 HOURS
INSTRUCTION	:	ANSWER **ALL** QUESTIONS

THIS QUESTION PAPER CONSISTS OF FIVE **(5)** PAGES

Q1 (a) Convert the following expressions from Postfix to Infix notation.

(i) $3\ 5\ 7 + 2\ 1 - \times 1 + +$
(ii) $12 + 3 + 4 + 5 + 6 + 7 +$
(iii) $ABCDE + F\ / + G - H / \times +$

(3 marks)

(b) Assume there are four microprocessors with different instruction format. Each microprocessor requires the following amount of time to fetch, decode, and execute each instruction as shown in **Table Q1(b)**. Which microprocessor is the fastest to perform the operation $A = B - C$ using Reduced Instruction Set Computing (RISC) instruction set?

Table Q1(b)

Microprocessor	Instruction Type	Time per instruction
CPU 0	Zero-address instructions	50 ns
CPU 1	One-address instructions	40 ns
CPU 2	Two-address instructions	80 ns
CPU 3	Three-address instructions	150 ns

(7 marks)

(c) Produce a RISC-type assembly program to evaluate the following arithmetic statement. Use only two registers in the program.

$$S = \frac{A + D}{B - 5} \times 7 + F\ /\ 2$$

(i) Three address instructions

(3 marks)

(ii) Two address instructions

(3 marks)

(d) Consider a CISC-style processor, create a program that computes the expression

$$X = Y8 + \mathrm{B} *$$

where $B = + - A2 * FC$ using two-address instruction format. Use only two registers in the program.

(4 marks)

Q2 (a) Describe the cycle for instruction execution.

(4 marks)

(b) Distinguish between Program-controlled I/O and Interrupt-driven I/O in terms of CPU operation.

(4 marks)

(c) Based on the block diagram shown in **Figure Q2(c)**, write step by step operations to execute the following instruction (consisting of fetch instruction/data, execute, and write back steps)

Add R10, R7, R31

using register transfer notation. Assume the last element in the assembly language notation is the destination.

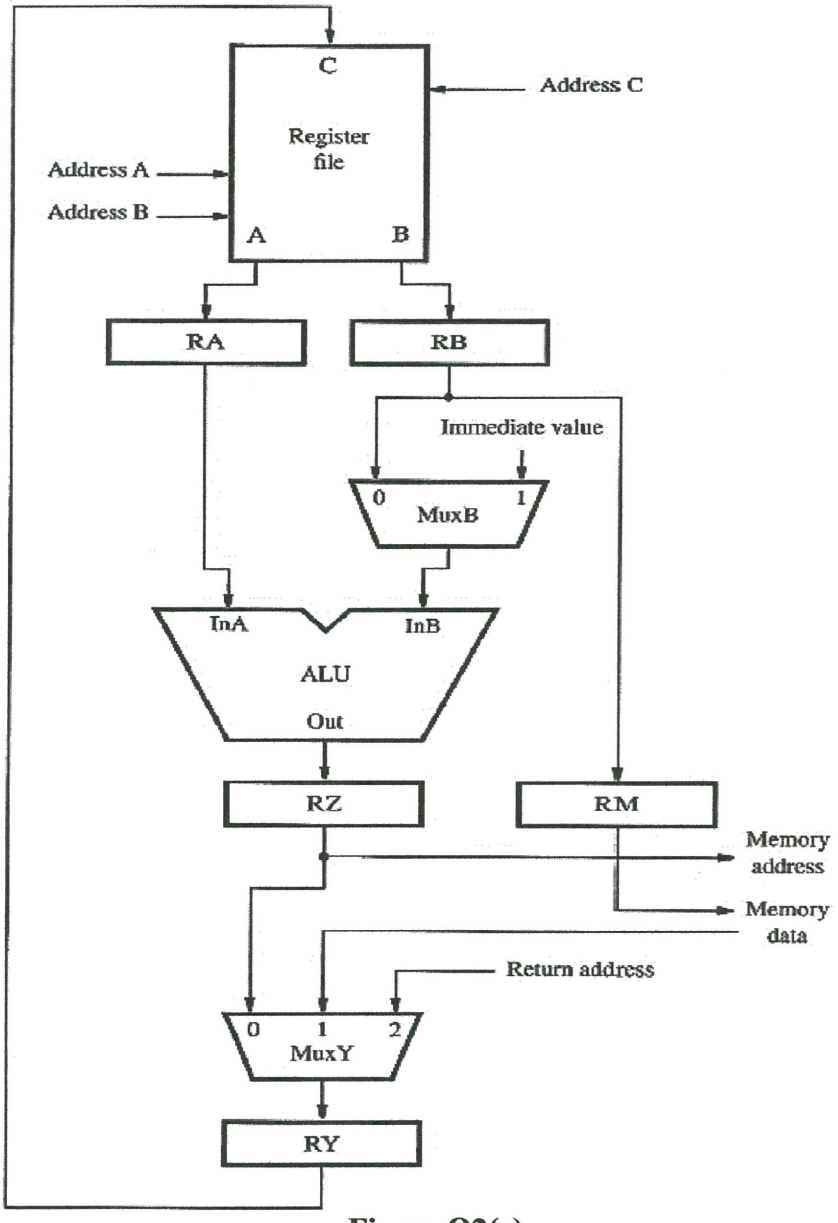

Figure Q2(c)

(12 marks)

Q3 (a)

(i) List two (2) types of electronic gadgets using USB protocol for their communication.

(2 marks)

(ii) Give reasons for electronic gadgets in adopting USB protocol?

(2 marks)

(b) Discuss the advantages and disadvantages of asynchronous bus.

(4 marks)

(c) Describe three (3) working principles of I/O interface for an input device.

(6 marks)

(d) Differentiate between interrupt-driven I/O, isolated I/O, and memory-mapped I/O.

(6 marks)

Q4 (a) Several instructions will be executed by Intel™ Xeon™ processor having 4-stage pipelined architecture. The instruction cycle comprises 4 steps; *fetch (F), decode (D), execute (E), and write back (W)*, where all steps require 1 clock cycle except the execute step, which takes 2 clock cycles. Assume *1 clock cycle = 5 ns*.

(i) Sketch the space time diagram to execute four (4) instructions.

(8 marks)

(ii) Calculate the total execution time (in *ns*) needed by the pipelined computer to execute a C++ program having 1500 instructions.

(4 marks)

(iii) Calculate the performance speed up of the pipelined computer over non-pipelined computer to execute similar C++ program in **Q4(a)(ii)**.

(4 marks)

(b) A non-pipeline system takes *50 ns* to process a task. The same task can be processed in a six segment pipeline with a clock cycle of *10 ns*.

(i) Determine the speed up ratio of the pipeline for 100 tasks.

(2 marks)

(ii) Compute the maximum speed up that can be achieved.

(2 marks)

Q5 (a) Differentiate the memory access time between primary storage and secondary storage.

(4 marks)

(b) Referring to **Figure Q5(b)**, describe the function of element X.

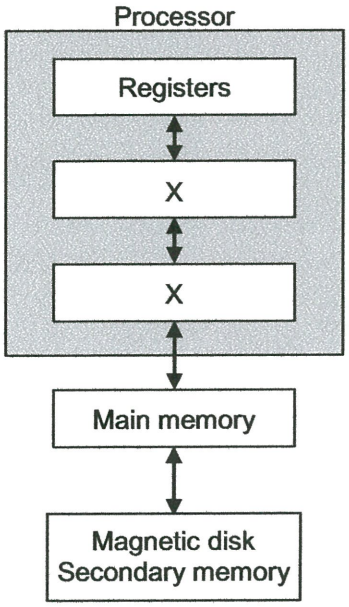

Figure Q5(b)

(4 marks)

(c) Reason why DRAM has higher storage density compared with SRAM using appropriate diagrams.

(8 marks)

(d) From **Table Q5(d)**, determine the miss penalty in *ns* when a L2 cache miss occurs. Assume *1 clock cycle = 10 ns*.

Table Q5(d)

Memory Level	Processor Clock Cycle (*ns*)
L1 cache	3
L2 cache	7
L3 cache	10
DDR SDRAM	100
Hard disk	150

(2 marks)

(e) Distinguish the principle of operation for SRAM and optical in terms of the way binary values are stored.

(2 marks)

– END OF QUESTIONS –