CONFIDENTIAL

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2016/2017

COURSE NAME	:	ELECTRONIC CIRCUITS ANALYSIS AND DESIGN
COURSE CODE	:	BEL 30403
PROGRAMME CODE	:	BEJ
EXAMINATION DATE	:	DECEMBER 2016 / JANUARY 2017
DURATION	:	3 HOURS
INSTRUCTION	:	ANSWERS **ALL** QUESTIONS

THIS QUESTION PAPER CONSISTS OF **NINE (9)** PAGES

CONFIDENTIAL

Q1 In October 2016, Jurutera Hati Suri Sdn Bhd has been awarded a project to design flood detector by Jabatan Pertahanan Awam Malaysia. To kickoff the project immediately, they plan to utilise operational amplifier as the fundamental component of their initial design.

(a) In the first design, the detector circuit is designed such that it

- recognises as low as 0.8 V of input voltage for flood warning, and
- produces 10 V when flood warning is activated, otherwise the output remains at -10 V

(i) Show a possible circuit design to satisfy the pre-defined outcomes mentioned in **Q1(a)**.

(4 marks)

(ii) Prove that, using input-output relationship diagram, the circuit design in **Q1(a)(i)** could achieve the prerequisite conditions mentioned in **Q1(a)**.

(6 marks)

(b) Next, the circuit in **Q1(a)** is modified such that the input voltage for flood warning is raised to Zener voltage of 1.2 V.

(i) Show a possible circuit design to satisfy the pre-defined outcomes mentioned in **Q1(b)**.

(4 marks)

(ii) Show the input-output waveform to prove that the circuit design in **Q1(b)(i)** could achieve condition mentioned in **Q1(b)**.

(6 marks)

Q2 In order to escalate competition in broadband services, the Malaysian Communications and Multimedia Commission (MCMC) has appointed Pening Lalat Sdn Bhd to operate 4G-LTE in a new band spectrum. The awarded spectrum is centred at 840 MHz with bandwidth of 20 MHz.

(a) As a leader of this project, design an active filter that could ensure that the transmitted signal will reach the end user within the specified band spectrum. The frequency response shall

- be maximally flat response,
- have roll-off not more than 20 dB/decade, and
- have gain not less than 50 dB.

(12 marks)

(b) Verify that the filter design in **Q2(a)** meets the requirement of your client, Pening Lalat Sdn Bhd in which you need to show:
- quality factor of filter, and
- a complete frequency response.

(8 marks)

Q3 In order to improve mobile communication in Parit Raja, Gegar Bagansa Sdn Bhd proposes a wider bandwidth of frequency band covered. The proposal put forward the block diagram of circuit changes as shown in **Figure Q3**. Gegar Bagansa Sdn Bhd claims the circuit being proposed could achieve the following:

- main purpose is to amplify the input voltage
- the closed-loop gain is at least 70% of the open-loop gain
- the open-loop gain, A, is not less than 1000.

(a) Design a feedback circuit as shown in **Figure Q3** by determining the circuit configuration and its corresponding attenuation (feedback network) value. Assume $A\beta \gg 1$.

(6 marks)

(b) Determine the following:

(i) ratio $\frac{Z_{if}}{Z_i}$

(ii) ratio $\frac{Z_{of}}{Z_o}$

(iii) ratio $\frac{BW_f}{BW}$

(iv) ratio $\frac{A_f}{A}$

(10 marks)

(c) Analyse the drawback of implementing the circuit design shown in **Figure Q3** related to mobile communication service in targeted area.

(4 marks)

Q4 As a design engineer in 1MAO Electronics, you are assigned to design an oscillator circuit that satisfies the following requirements:

- the output signal has 0° phase shift
- frequency of oscillation at 500 Hz

(a) Propose a circuit design that meets the requirements by showing:
- values of all required components
- a complete circuit configuration

(12 marks)

(b) Predict the possible output waveform and analyse its related application. Support your answer by showing input-output waveform and the corresponding gain.

(8 marks)

Q5 (a) **Figure Q5(a)** is a full wave bridge circuit with a capacitor filter. Given capacitor, C = 1000 μF, DC current, I_{dc} = 0.1 A and forward diode voltage, V_{diode} = 0.7 V.

(i) Calculate the peak voltage at secondary winding, $V_{p(sec)}$, output average voltage, V_{dc} and peak-to-peak ripple voltage, $V_{r(p\text{-}p)}$

(6 marks)

(ii) Draw the output waveforms of V_{sec} and V_{o}.

(4 marks)

(b) An additional RC filter is connected to the circuit in **Figure Q5(a).** Compare and conclude on the old and new ripple factor (%) if the value R and C are 50 Ω and 100 μF, respectively. Use R_L = 100 Ω.

(6 marks)

(c) Determine the minimum and maximum output voltages for voltage regulator in **Figure Q5(c)** if given R_1 = 200 Ω, R_2 = 5 kΩ. Assume I_{ADJ} = 50 μA and V_{ref} = 1.5 V.

(4 marks)

- END OF QUESTIONS –

FINAL EXAMINATION

SEMESTER / SESSION : SEM I / 2016/2017
COURSE NAME : ELECTRONIC CIRCUITS ANALYSIS AND DESIGN
PROGRAMME CODE : BEJ
COURSE CODE : BEL 30403

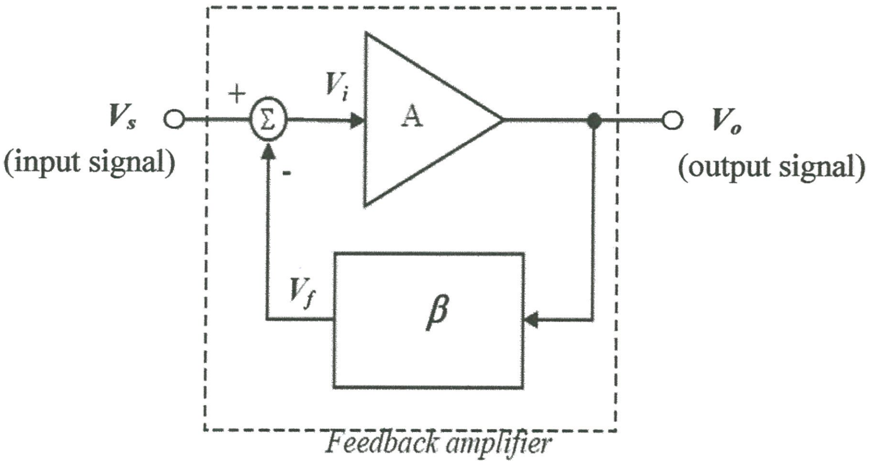

Figure Q3

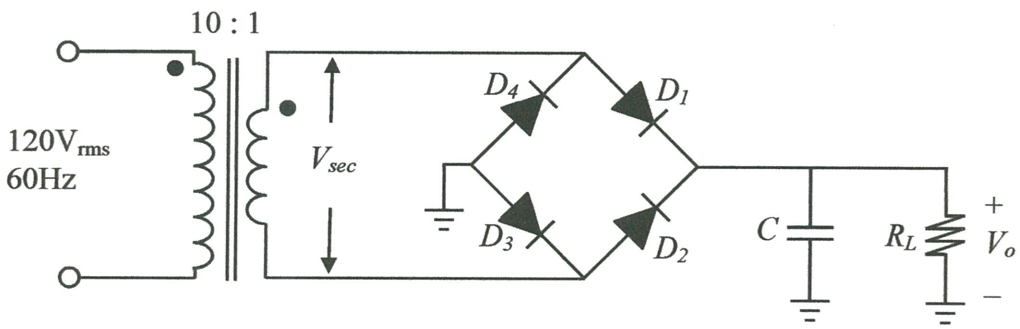

Figure Q5(a)

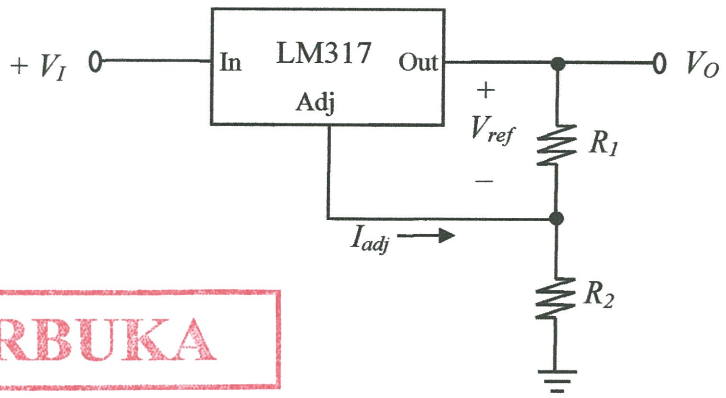

Figure Q5(c)

FINAL EXAMINATION

SEMESTER / SESSION : SEM I / 2016/2017
COURSE NAME : ELECTRONIC CIRCUITS ANALYSIS AND DESIGN
PROGRAMME CODE : BEJ
COURSE CODE : BEL 30403

Table 1 List of formula

Inverting Amplifier	$A_V = \frac{V_o}{V_i} = -\frac{R_f}{R_1}$
Non-Inverting Amplifier	$A_V = \frac{V_o}{V_i} = 1 + \frac{R_f}{R_1}$
Inverting Summing Amplifier	$V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right)$
Non-Inverting Summing Amplifier	$V_o = \left(1 + \frac{R_f}{R_1}\right)\left(\frac{R_B}{R_A + R_B}V_A + \frac{R_A}{R_A + R_B}V_B\right)$
Subtracting Amplifier	$V_o = \left(1 + \frac{R_f}{R_1}\right)\left(\frac{R_3}{R_2 + R_3}V_2 - \frac{R_f}{R_1 + R_f}V_1\right)$
Instrumentation Amplifier	$A_T = A_1 A_2 = \frac{v_o}{v_{in}} = \left(1 + \frac{2R}{R_x}\right)\left(\frac{R_4}{R_3}\right)$
Integrator	$V_o(t) = -\frac{1}{RC}\int_{t_0}^{t_1} V_i(t)\,dt + V_o(t_0)$
Differentiator	$V_o(t) = -RC\frac{dV_i(t)}{dt}$
Schmitt Trigger	$V_{UTP \text{ or } LTP} = \frac{R_2}{R_1 + R_2}(\pm V_{out(\max)}) + \frac{R_1}{R_1 + R_2}(V_{REF})$
Cut-off frequency for a filter	$f_c = \frac{1}{2\pi RC}$
1st order Low Pass Filter	$A_V(s) = \frac{V_o}{V_i} = \left(1 + \frac{R_F}{R_1}\right)\left(\frac{1}{1 + sRC}\right)$
2nd order Low pass filter	$A_V(s) = \frac{V_o}{V_i}(s) = \frac{A_{VO}}{(RCs)^2 + (3 - A_{VO})RCs + 1}$
1st order High Pass Filter	$A_V(s) = \frac{V_o}{V_i} = \left(1 + \frac{R_F}{R_1}\right)\left(\frac{1}{1 + \frac{1}{sRC}}\right)$

FINAL EXAMINATION

SEMESTER / SESSION : SEM I / 2016/2017
COURSE NAME : ELECTRONIC CIRCUITS ANALYSIS AND DESIGN
PROGRAMME CODE : BEJ
COURSE CODE : BEL 30403

Table 1 List of formula (Cont..)

2nd order High Pass Filter	$A_V(s)=\frac{V_O}{V_i}(s)=\frac{A_{VO}}{\frac{1}{(sRC)^2}+\frac{3-A_{VO}}{sRC}+1}$
Negative feedback – Gain	$A_f=\frac{V_o}{V_S}=\frac{A}{1+\beta A}$
Positive feedback – Gain	$A_f=\frac{A}{1-\beta A}$
Phase shift oscillator	$\beta=\frac{V_F}{V_o}=\frac{1}{\left(1-\frac{5}{\omega^2R^2C^2}\right)+j\left(\frac{1}{\omega^3R^3C^3}-\frac{6}{\omega RC}\right)}$ or $\beta=\frac{V_F}{V_o}=\frac{1}{\left(1-5\omega^2R^2C^2\right)+j\left(6\omega RC-\omega^3R^3C^3\right)}$ $f_o=\frac{1}{2\pi RC\sqrt{6}}$ or $f_o=\frac{\sqrt{6}}{2\pi RC}$
Wien bridge oscillator	$f_o=\frac{1}{2\pi\sqrt{R_1R_2C_1C_2}}$
Colpitts Oscillator	$f_o=\frac{1}{2\pi\sqrt{LC_{eq}}}$ $C_{eq}=\frac{C_1C_2}{C_1+C_2}$
Hartley Oscillator	$f_o=\frac{1}{2\pi\sqrt{CL_{eq}}}$ $L_{eq}=L_1+L_2$
UJT relaxation oscillator	$f_o=\frac{1}{R_TC_T\ln[1/(1-\eta)]}$
Square-wave Oscillator	$f=\frac{1}{T}=\frac{1}{2RC\ln\left(\frac{1+\beta}{1-\beta}\right)}$ $\beta=\frac{R_3}{R_3+R_2}$

FINAL EXAMINATION

SEMESTER / SESSION : SEM I / 2016/2017
COURSE NAME : ELECTRONIC CIRCUITS ANALYSIS AND DESIGN
PROGRAMME CODE : BEJ
COURSE CODE : BEL 30403

Table 1 List of formula (Cont..)

Triangular-wave Oscillator	$f = \frac{1}{4R_1C}\frac{R_2}{R_3}$
Capacitor voltage	$v_c(t) = v_c(0) + \left(v_c(\infty) - v_c(0)\right)\left(1 - e^{-t/\tau}\right)$ $= v_c(\infty) + \left(v_c(0) - v_c(\infty)\right)e^{-t/\tau}$
Astable Multivibrator	$T_m = t_1 = \tau_2 \ln 2 = 0.693(R_1 + R_2)C_1$ $T_s = t_2 = \tau_2 \ln 2 = 0.693 R_2 C_1$ $T = T_m + T_s$ $f = \frac{1.44}{(R_1 + 2R_2)C_1}$ $D = \frac{T_m}{T_m + T_s} \times 100\% = \frac{R_1 + R_2}{R_1 + 2R_2} \times 100\%$
Monostable Multivibrator	$T = 1.1\, R_1 C_1$
Ripple Factor	$\% r = \frac{\text{ripple voltage (rms)}}{\text{dc voltage}} = \frac{V_{r(rms)}}{V_{dc}} \times 100$
Half-wave rectifier with a filter	$V_{r(rms)} = \frac{V_{r(p-p)}}{2\sqrt{3}} \approx \frac{V_{o(p)}}{2\sqrt{3} f C R_L}$ $V_{o(DC)} = V_{o(p)} - \frac{V_{r(p-p)}}{2}$ $\quad V_{r(p-p)} \approx \frac{V_{o(p)}}{fCR_L} = \frac{I_{o(DC)}}{fC}$ $r = \frac{V_{r(rms)}}{V_{DC}} \approx \frac{1}{2\sqrt{3} f C R_L}$
Full-wave rectifier with a filter	$V_{r(rms)} = \frac{V_{r(p-p)}}{2\sqrt{3}} \approx \frac{V_{o(p)}}{4\sqrt{3} f C R_L} = \frac{I_{DC}}{4\sqrt{3} f C}$ $V_{o(DC)} = V_{o(p)} - \frac{V_{r(p-p)}}{2}$ $V_{r(p-p)} = \frac{I_{o(DC)}}{2fC} \approx \frac{V_{o(p)}}{2 f C R_L}$

FINAL EXAMINATION

SEMESTER / SESSION : SEM I / 2016/2017
COURSE NAME : ELECTRONIC CIRCUITS ANALYSIS AND DESIGN
PROGRAMME CODE : BEJ
COURSE CODE : BEL 30403

Table 1 List of formula (Cont..)

	$r = \frac{V_{r(rms)}}{V_{DC}} \approx \frac{1}{4\sqrt{3} f C R_L}$
Rectifier with Additional RC filter	$V'_{r(rms)} \approx \frac{X_C}{R} V_{r(rms)}$
Inductor Filter	$r = \frac{R_L}{3\sqrt{2}\omega L}$
Shunt regulator	$V_o \cong V_B \left(\frac{R_1 + R_2}{R_2} \right)$ $V_B = V_Z + V_{BE}$ $V_o \cong \left(\frac{R_1 + R_2}{R_2} \right)(V_Z)$
Series regulator	$V_o = \frac{R_1 + R_2}{R_1}(V_Z + V_{BE})$ $V_o = V_Z \left(\frac{R_1 + R_2}{R_1} \right)$
Adjustable IC regulator	$V_o = V_{ref} \left(1 + \frac{R_2}{R_1} \right) + I_{adj} R_2$