

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION SEMESTER I **SESSION 2016/2017**

COURSE NAME

: ANALOG ELECTRONICS

COURSE CODE

: BEL10203

PROGRAMME : BEJ/BEV

EXAMINATION DATE : DECEMBER 2016/JANUARY 2017

DURATION

: 3 HOURS

INSTRUCTION

: ANSWER ALL QUESTIONS



THIS QUESTION PAPER CONSISTS OF EIGHT (8) PAGES

Q1 (a) Describe in your own words and construct a diagram to explain the conditions established by forward-bias and reverse-bias on a non-ideal p-n junction diode with barrier potential, $V_F=0.7\ V$ and breakdown voltage, $V_{BR}=-20\ V$; and how the resulting currents are affected.

(5 marks)

- (b) Analyze circuit in Figure Q1(b) carefully. Calculate value of the following,
 - (i) Current i_1 .

(2 marks)

(ii) Current i_2 .

(2 marks)

(iii) Current i_3 .

(2 marks)

(c) Briefly explain the Q-point in diode application by the aid of diagram.

(3 marks)

(d) Design a clamper to perform the function indicated in **Figure Q1(d)**.

(6 marks)

- **Q2 Figure Q2** shows a common emitter voltage divider bias amplifier with unbypassed R_E and load, R_L . Given $R_I = 15$ kΩ, $R_2 = R_L = 3.3$ kΩ, $R_C = 3.9$ kΩ, $R_E = 1$ kΩ, $\beta = 100$, $V_{CC} = 15$ V and assume $V_{BE} = 0.7$ V. Show all the calculation clearly.
 - (a) Identify TWO (2) purposes of coupling capacitor in Figure Q2.

(4 marks)

(b) Draw the Alternating Current (AC) equivalent circuit using r_e model. Assume $r_o = \infty$

(3 marks)

(c) Calculate the input impedance, Z_i and output impedance, Z_o . (Hint: Check the testing condition and relates with Direct Current (DC) analysis if required).

(7 marks)

TERBUKA

CONFIDENTIAL

(d) Calculate the voltage gain, A_v and the current gain, A_i . (4 marks)

(e) State ONE (1) advantage of common emitter circuit.

(2 marks)

- Q3 (a) An emitter-bias configuration of Figure Q3(a) has $V_{CC} = 12 \text{ V}$, $V_C = 7.6 \text{ V}$, $V_E = 2.4 \text{ V}$, $I_C = 2 \text{ mA}$ and $\beta = 80$. If current flow in the emitter is assumed approximately equal to the collector current,
 - (i) determine the resistor of R_C .

(2 marks)

(ii) determine the resistor of R_E .

(1 mark)

(iii) determine the resistor of R_B .

(3 marks)

(iv) calculate the voltage of V_B .

(1 mark)

- (b) An emitter voltage divider bias configuration of **Figure Q3(b)** has $R_C = 3.9 \text{ k}\Omega$, $R_E = 0.68 \text{ k}\Omega$, $R_I = 62 \text{ k}\Omega$, $R_2 = 9.1 \text{ k}\Omega$ and $\beta = 80$. If the $V_{CC} = 16 \text{ V}$ and the current flow in the emitter is assumed approximately equal to the collector current,
 - (i) evaluate the suitable approach in analyze the circuit.

(2 marks)

(ii) determine the current of I_B .

(5 marks)

(iii) determine the voltage of V_{CE} .

(3 marks)

(c) State **THREE** (3) advantages of a Field Effect Transistor (FET) compared to a Bipolar Junction Transistor (BJT) analog component

(3 marks)

TERBUKA

- **Q4** Figure Q4(a) is an amplifier circuit that only amplifies the signals of specified frequencies. Assume that the Bipolar Junction Transistor (BJT) has an infinite value of Alternating Current (AC) collector resistance, r_o and gain current, $\beta = 120$:
 - (a) calculate the mid-band gain of this amplifier.

(6 marks)

(b) draw the low frequency AC equivalent circuit and determine the dominant low cut-off frequency.

(10 marks)

(c) sketch the normalized magnitude response of this filter. Clearly indicate the low cut-off frequency in this diagram.

(4 marks)

- Q5 (a) A push pull Class B amplifier is providing a 40 V peak to peak signal to a 16 Ω load (speaker) and power supplies of $V_{CC} = \pm 30$ V, determine:
 - (i) the input (DC) power, $P_i(dc)$.

(3 marks)

(ii) the output (AC) power, $P_o(ac)$.

(3 marks)

(iii) circuit efficiency.

(3 marks)

(iv) power dissipated by each output transistor

(3 marks)

(b) Class AB usually found in low frequency amplifier system. Suggest **TWO (2)** applications using Class AB Amplifier.

(4 Marks)

(c) List **TWO (2)** advantages of Class AB amplifier compared to class A and B.

(4 Marks)



-END OF QUESTIONS-

CONFIDENTIAL

SEMESTER/SESSION: SEM I / 2016/2017

PROGRAMME: BEJ/BEV

COURSE NAME

: ANALOG ELECTRONICS

COURSE CODE: BEL 10203

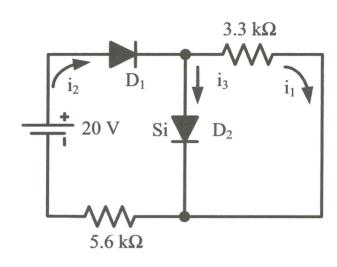


Figure Q1(b)

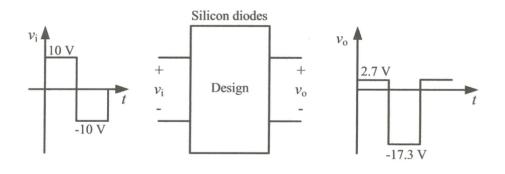


Figure Q1(d)



SEMESTER/SESSION: SEM I / 2016/2017

PROGRAMME: BEJ/BEV

COURSE NAME

: ANALOG ELECTRONICS

COURSE CODE: BEL 10203

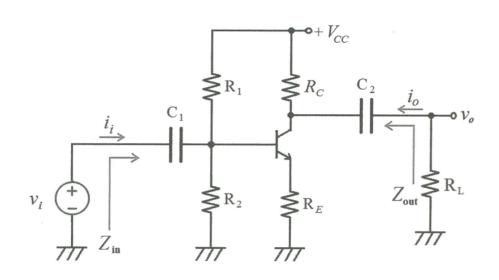


Figure Q2

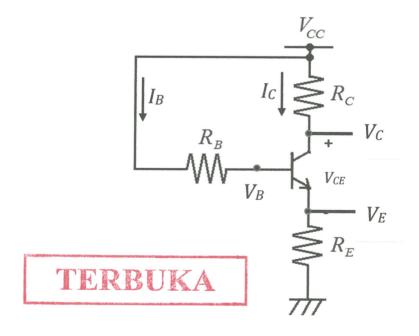


Figure Q3(a)

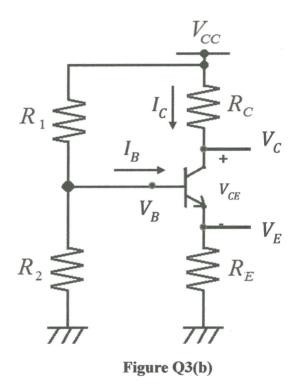
SEMESTER/SESSION: SEM I / 2016/2017

PROGRAMME: BEJ/BEV

COURSE NAME

: ANALOG ELECTRONICS

COURSE CODE: BEL 10203



TERBUKA

SEMESTER/SESSION: SEM I / 2016/2017

PROGRAMME: BEJ/BEV

COURSE NAME

: ANALOG ELECTRONICS

COURSE CODE: BEL 10203

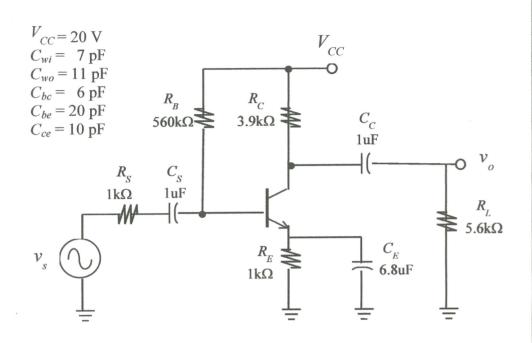


Figure Q4

TERBUKA