Universiti Tun Hussein Onn Malaysia

# UNIVERSITI TUN HUSSEIN ONN MALAYSIA

## FINAL EXAMINATION
## SEMESTER I
## SESSION 2016/2017



| | |
|---|---|
| COURSE NAME | : DIGITAL TECHNIQUES |
| COURSE CODE | : BEF12302 |
| PROGRAMME CODE | : BEV |
| EXAMINATION DATE | : DECEMBER 2016/ JANUARY 2017 |
| DURATION | : 2 HOURS |
| INSTRUCTION | : 1. ANSWER **ALL** QUESTIONS |
| | 2. ATTACH **APPENDIX A AND B** WITH YOUR ANSWER BOOKLET |

THIS QUESTION PAPER CONSISTS OF **ELEVEN (11)** PAGES

**Q1** (a) List **one (1)** disadvantage of series and parallel digital data transmission.

(2 marks)

(b) Identify why digital data transmission is preferred over analogue data transmission?

(4 marks)

(c) Convert the Gray code 111011000110 to BCD number.

(6 marks)

(d) Convert $324.253_{10}$ to octal.

(6 marks)

(e) A 4-bit binary number is represent by $A_3\ A_2\ A_1\ A_0$ with $A_3\ A_2\ A_1$ and $A_0$ are the individual bits and $A_0$ is the LSB. Draw a combinational logic circuit which produce an output HIGH when the binary number $A_3\ A_2\ A_1\ A_0$ should be at least $5_{10}$ and above and less than $12_{10}$.

(7 marks)

**Q2** (a) Simplify using Boolean Algebra:

(i) $\overline{AB + AC} + \overline{ABC}$.

(3 marks)

(ii) $(A + C)(A + \overline{B})$.

(3 marks)

(b) **Table 2 (b)** shows a truth table of a four-input and two-output logic function. Use Karnaugh maps, formulate:

(i) the minimal sum-of-product (MSOP) of expression for Y.

(5 marks)

(ii) the minimal product-of-sum (MPOS) of expression for Z.

(5 marks)

(c) A NAND gate is known as a universal gate as it can be configured into any basic logic gate.

i) Illustrate how a NAND gate can be used as OR gate.

(3 marks)

ii) Implement the function $Z = P\overline{Q} + \overline{S} + P\overline{R}$ using only a 2-input NAND gates.

(6 marks)

**Q3** (a) Explain the operation of the following functional combinational logic circuit. You may use appropriate diagram to aid your explanation.

i) Decoder.

(2 marks)

ii) Comparator

(2 marks)

(b) Analyze the 16 inputs multiplexer shown in **Figure Q3 (b)**.

i) Give brief explanation of the system.

(4 marks)

ii) Find the Boolean expression for the output Z

(6 marks)

(c) Implement the following Boolean expression using IC 74LS138 (3-to-8 decoder) in **APPENDIX A**. Symbol for IC 74LS138 is shown in **APPENDIX A** for the internal circuitry and pins assignment of 74LS138 (3-to-8 decoder).

$$Z = (\overline{A.B}) + (\overline{B + C})$$

(6 marks)

(d) Analyze the flip-flop circuit in **Figure Q3 (d)** and sketch output waveform. Assume both SET and CLR are inactive. Complete the timing diagram for Q in **APPENDIX B** and write down the operation (e.g. HOLD) that takes place in each clock pulse as illustrated in the diagram.

(5 marks)

**Q4** (a) Explain **one (1)** advantage and **two (2)** disadvantages of a synchronous counter compared to asynchronous counter.

(3 marks)

(b) **Figure Q4 (b)** shows the state transition diagram of a state machine.

(i) Build the excitation table for this state machine. Use JK flip-flops.

(10 marks)

(ii) Express the simplest Boolean expression for the circuit using Karnaugh map.

(6 marks)

(iii) Draw the circuit.

(4 marks)

(d) Explain the operation of the Parallel In Serial Out register (PISO) register. You may use appropriate diagram to aid your explanation.

(2 marks)

**-END OF QUESTION-**

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**Table 2 (b)**

| INPUT | | | | OUTPUT | |
|---|---|---|---|---|---|
| A | B | C | D | Y | Z |
| 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | X | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | X |
| 1 | 0 | 0 | 1 | X | 0 |
| 1 | 0 | 1 | 0 | X | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | X |
| 1 | 1 | 1 | 0 | X | 0 |
| 1 | 1 | 1 | 1 | X | 1 |

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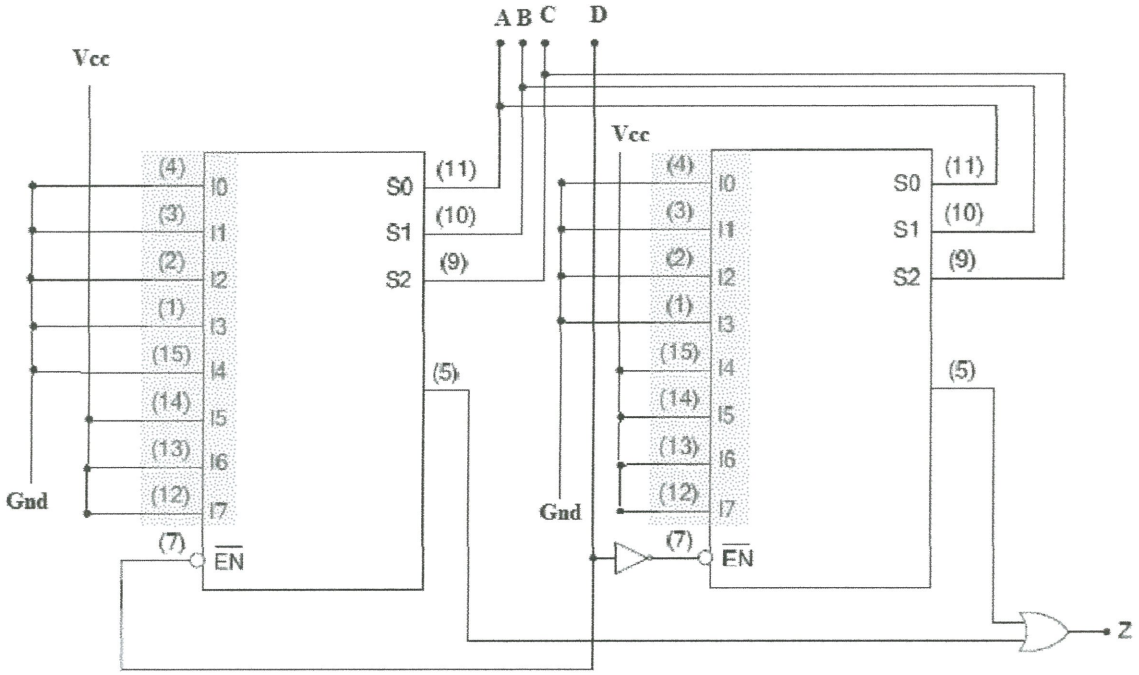


**FIGURE Q3 (b)**

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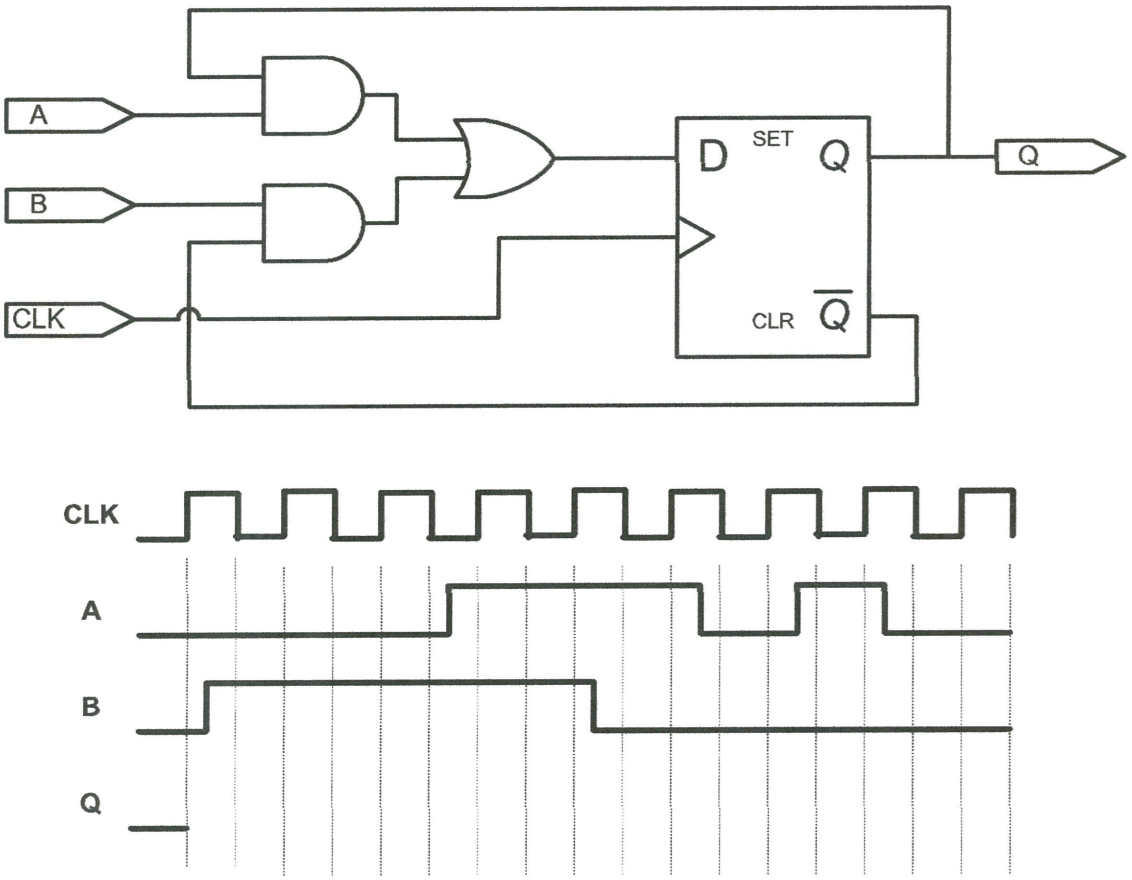





**FIGURE Q3 (d)**

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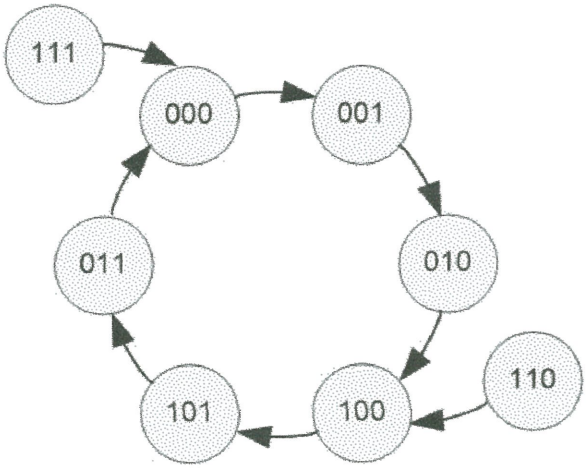


**FIGURE Q4 (b)**

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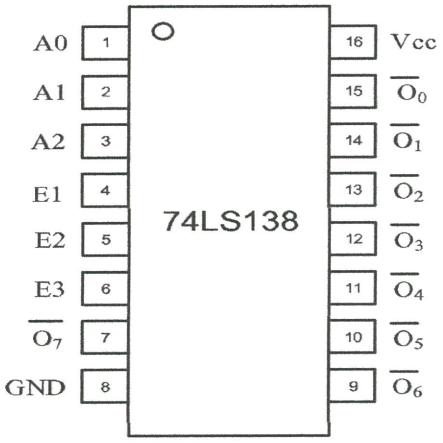
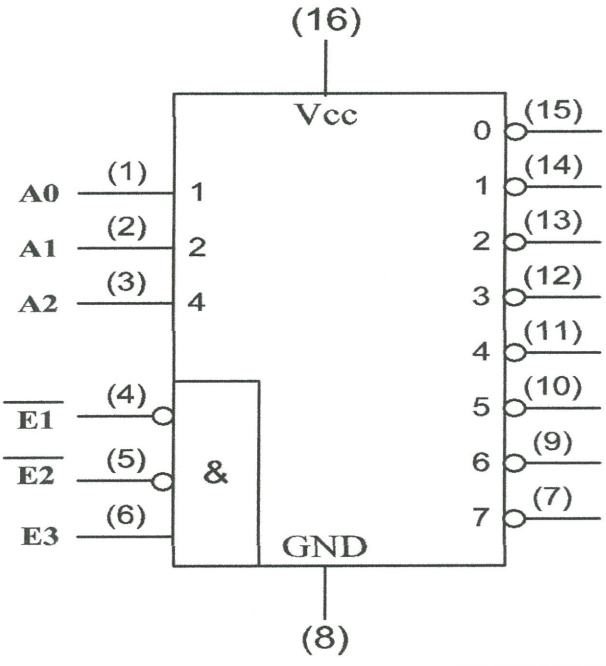
# APPENDIX A

## PIN ASSIGNMENT AND INTERNAL CIRCUITRY

### 74LS138 (3-to-8 Decoder)



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# APPENDIX B