UTHM
Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2016/2017

COURSE NAME	:	DIGITAL IC DESIGN
COURSE CODE	:	BED 30203
PROGRAMME	:	BACHELOR OF ELECTRONIC ENGINEERING WITH HONOURS
EXAMINATION DATE	:	DECEMBER 2016 / JANUARY 2017
DURATION	:	3 HOURS
INSTRUCTION	:	ANSWER **ALL** QUESTIONS

THIS QUESTION PAPER CONSISTS OF **FOUR (4)** PAGES

Q1 (a) Using an appropriate example, demonstrate how transistor scaling technology could improve the performance of a processor.

(5 marks)

(b) A digital circuit takes 2-bit numbers A and B as input and generates output Z as follows:
If A and B are odd numbers then Z=0,
If A and B are even numbers then Z=1,
If A is an even number and B is an odd number then Z=0,
If A is an odd number and B is an odd number then Z= X (don't care)

(i) Build the truth table and acquire the minimum Boolean expression for Z.

(4 marks)

(ii) Design a complete transistor-level circuit diagram to realize the equation obtained in **Q1(b)(i)** using a fully complementary static CMOS logic with minimum number of transistor. Assume that all inverted inputs are available. Clearly label the designed circuit.

(6 marks)

(iii) Propose the most compact stick diagram layout circuit in **Q1(b)(ii)**. Draw and completely label the stick diagram.

(6 marks)

(c) **Figure Q1(c)** shows the transmission gate configuration for function Z. Analyse and obtain the Boolean expression for Z.

(4 marks)

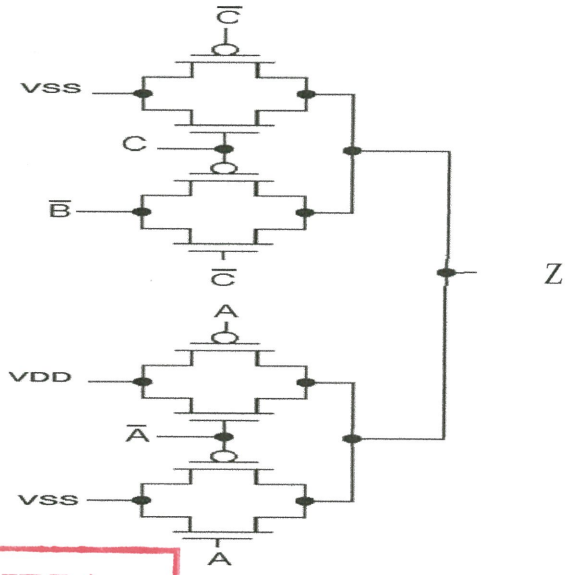

Figure Q1(c)

Q2 (a) Propose and justify a modification to transistors dimension that could increase their performance.

(6 marks)

(b) Deduce the effect of notch in power lines (VDD and VSS).

(4 marks)

(c) Design rules are the rules that have to be respected when a given design is laid out. Discuss how process design rule could improve **TWO (2)** points of concern in IC design: circuit safety and circuit reliability. Give the appropriate design rule with related diagram to support your discussion.

(12 marks)

(d) Discuss the purpose of having a complete layout floorplan in design implementation process.

(3 marks)

Q3 (a) System-on chip (SOC) is a type of integrated circuit that incorporates multiple functions in a single chip. Discuss how SOC design flow could achieved an effective design flow criterion.

(8 marks)

(b) Analyse the needs of synthesising the RTL code in ASIC design flow.

(6 marks)

(c) Standard cells are normally used in full custom design in order to speed up design process. Demonstrate the essential characteristic of standard cells that could reduce the design time cycle significantly.

(6 marks)

(d) Every chip communicates with external world through wire bonding to pad cells of chip. With the aid of a diagram, discuss **TWO (2)** important requirements of pad cells to ensure a reliable chip connection.

(4 marks)

Q4 (a) Electromigration is the unwanted movement of materials in a semiconductor that can lead to the electrical failure of interconnects in relatively short times, reducing the circuit lifetime to an unacceptable level. Propose a technique to prevent an electromigration problem in the power lines.

(5 marks)

(b) Two approaches of clock signal routing in layout design are single clock signal and clock tree. Analyse the implementation in the clock tree approach for delay improvement.

(6 marks)

(c) Explain **TWO (2)** importance of clock shielding in clock signal routing in circuit design.

(4 marks)

(d) A trend in microprocessor design is operating frequency increment to improve its performance. Deduce that this approach has negative impact on circuit reliability in the long run.

(4 marks)

(e) Discuss **THREE (3)** purposes of power routing in circuit design.

(6 marks)

- END OF QUESTION -