Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2016/2017

COURSE NAME	:	DIGITAL DESIGN
COURSE CODE	:	BEC 30503
PROGRAMME CODE	:	BEJ
EXAMINATION DATE	:	DECEMBER 2016 / JANUARY 2017
DURATION	:	3 HOURS
INSTRUCTION	:	ANSWERS ALL THE QUESTIONS

THIS QUESTION PAPER CONSISTS OF **SEVEN (7)** PAGES

Q1 (a) Discuss TWO (2) goals of technology scaling down in IC design.

(4 marks)

(b) A lot of problems occur while shrinking down IC scale. Recommend TWO (2) solutions for following problems:

(i) interconnect area

(4 marks)

(ii) complicated design

(4 marks)

(c) Explain the advantages of using FPGAsover ASICs.

(4 marks)

(d) Rosmah has designed a crafty circuit for counting raindrops. She decides to sell the device and try make some money, but she needs help deciding what implementation to use. She decides to use either an FPGA or an ASIC. The development kit to design and test the FPGA costs $1500. Each FPGA costs $17. The ASIC costs $600,000 for a mask set and $4 per chip.

Regardless of what chip implementation she chooses, Rosmah needs to mount the packaged chip on a printed circuit board (PCB), which will cost her $1.50 per board. She thinks she can sell 1000 devices per month. Rosmah has coerced a team of bright undergraduates into designing the chip for their senior project, so it doesn't cost her anything to design.

If the sales price has to be twice the cost (100% profit margin), and the product life is 2 years, which implementation is the better choice?Justify your answer.

(4 marks)

Q2 (a) Sketch a general design flow for configuring an FPGA.

(4 marks)

(b) Give TWO (2) reasons why logic synthesis using HDL is the state-of-the-art method to model and design digital hardware.

(4 marks)

(c) The simulation process is used to verify the correctness of the design.

(i) List two (2) types of simulation.

(2 marks)

(ii) Describe the difference between the simulations in Q2(c)(i).

(2 marks)

(d) Write an HDL code using CASE statement to describe a 2-line to 4-line decoder with an enable input. The decoder's function table is shown in **Table Q2(d)**.

Table Q2(d)

Inputs			Outputs			
EN	B	A	Y3	Y2	Y1	Y0
0	x	x	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

(8 marks)

Q3 (a) **Figure Q3(a)** shows a 1-bit comparator, which is used to compare the two 1-bit inputs, A and B. If A equal to B, the comparator generates a logic "1", otherwise a logic "0".

(i) Describea 1-bit comparator circuit in **Figure Q3(a)** using gate level modelling.

(5 marks)

(ii) You are required to modify the 1-bit comparator to be a 2-bit comparator. Illustrate the construction of 2-bit comparator from 1-bit comparator.

(4 marks)

(iii) Write the HDL behavioral code for 2-bit comparator.

(5marks)

(b) A room in a smart home has a cooler and a fan, each havingits own switch. The fan is controlled by an additional logic.If the cooler is ON and the temperature is below 30 degrees,the fan will remain off. Write a HDL behavioral code to model this circuit.

(6 marks)

Q4 (a) Define the terms "optimization" and "tradeoff".

(4 marks)

(b) Given the logic gate library in **Figure Q4(b)(i)**, optimize the circuit in **Figure Q4(b)(ii)** to reduce power consumption without increasing the circuit's delay.

(6 marks)

(c) Write HDL code to implement the RTL schematic shown in **Figure Q4(c)**.

(10 marks)

Q5 (a) **Figure Q5(a)** shows a finite state machine diagram. Determine thetype of finite state machine.

(2 marks)

(b) Constructa behavioral HDL code that implements **Figure Q5(a)**. Your code should use a single behavior for the state register, next-state logic, and output logic. Use the signal or register names and state assignment given on the graph.

(10 marks)

(c) **Figure Q5(c)** shows an example of ASM chart for up down counter.

(i) Explain why the designer use the ASM chart.

(2 marks)

(ii) Describe THREE (3) basic elements used in an ASM chart.

(6 marks)

-END OF QUESTIONS -

FINAL EXAMINATION

SEMESTER / SESSION : I / 2016/2017 PROGRAMME CODE : BEJ
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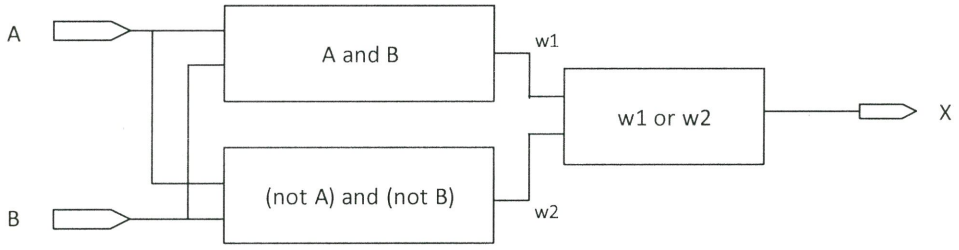

Figure Q3(a)

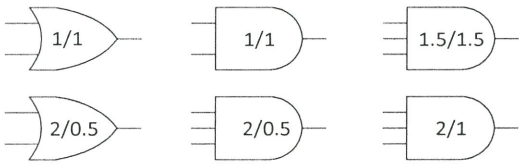

Figure Q4(b)(i)

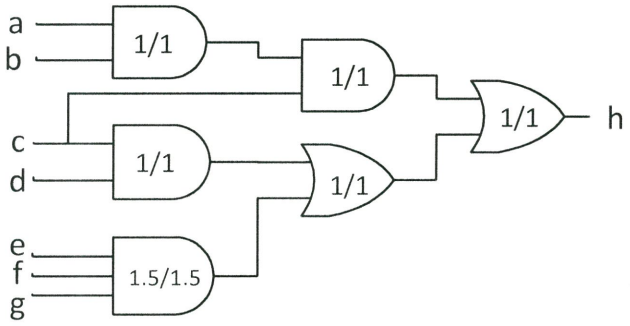

Figure Q4(b)(ii)

FINAL EXAMINATION

SEMESTER / SESSION : I / 2016/2017 PROGRAMME CODE : BEJ
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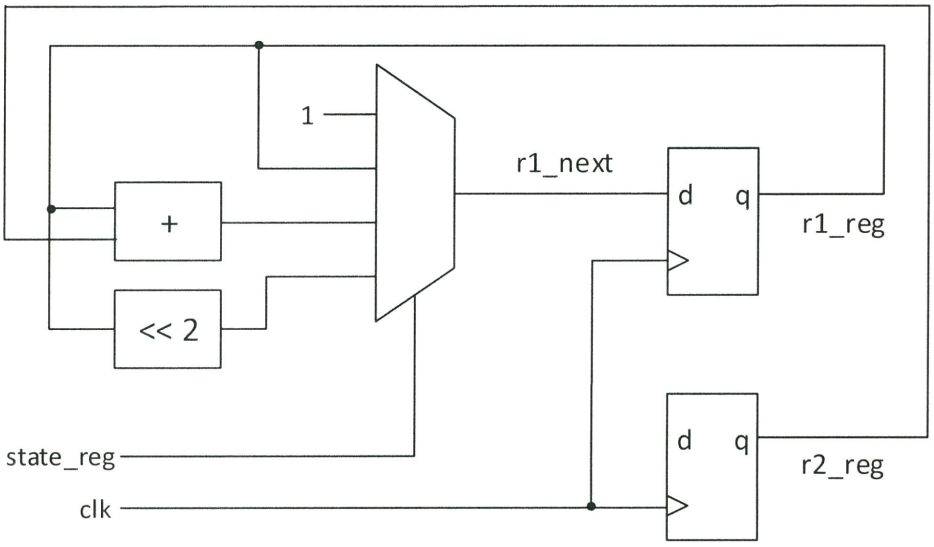

Figure Q4(c)

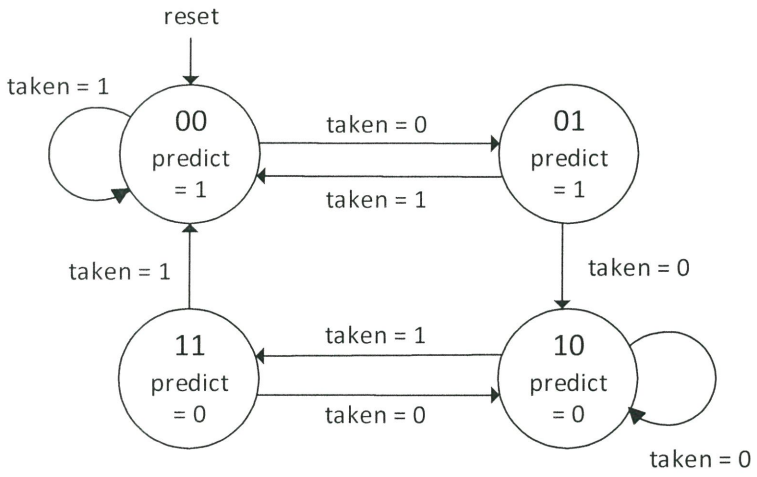

Figure Q5(a)

FINAL EXAMINATION

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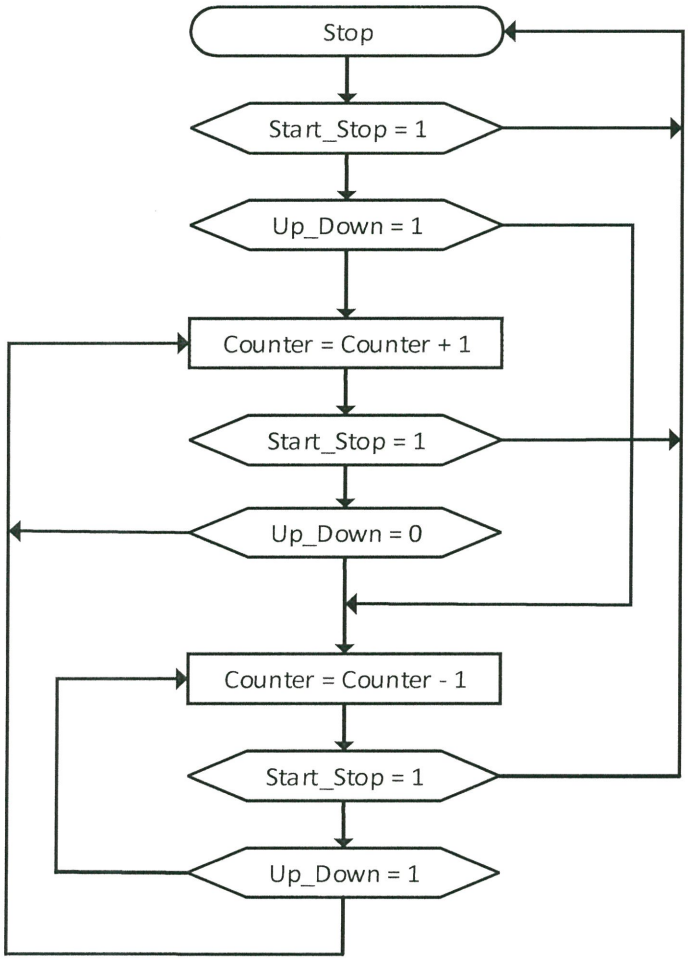

Figure Q5(c)