Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2015/2016

COURSE NAME	: ADVANCED MICROCONTROLLER
COURSE CODE	: BEC 41103
PROGRAMME CODE	: BEJ
EXAMINATION DATE	: JUNE / JULY 2016
DURATION	: 3 HOURS
INSTRUCTION	: ANSWER **ALL** QUESTIONS

THIS QUESTION PAPER CONSISTS OF **FIFTEEN (15)** PAGES.

Q1 (a) **Figure Q1(a)** illustrates pin diagram of 40-pin DIP package for PIC18F4420 and PIC18F4520 microcontrollers.

(i) How many PORTs available for I/O operations. List all of them.

(2 marks)

(ii) How many pins are designated as I/O port pins.

(2 marks)

(iii) Explain the role of TRISx and PORTx in I/O operations.

(4 marks)

(b) In **Figure Q1(b)**, assume the switch connected to RB7 is an emergency switch. Write a program to read RB7, and if it is on (grounded), flash the LED connected to RB6 at every 100ms interval (assume that DELAY_100ms subroutine is available).

(12 marks)

Q2 (a) A free-running 16-bit timer has a clock frequency 5MHz. The counter register in the timer is incremented every clock cycle. When the counter reaches FFFFH, it rolls over to 0000 and continues to count.

(i) Find the frequency and period used by the timer.

(4 marks)

(ii) If the timer reading at the beginning of the event is 1FF8H and at the end of the event is 3380H, calculate the time delay between the two events.

(4 marks)

(b) **Figure Q2(b)** shows Timer3 block diagram.

(i) Give the highest size of prescaler supported by Timer3.

(2 marks)

(ii) Justify whether the Timer3 supports event counter.

(3 marks)

(iii) Specify operation modes available in Timer3.

(2 marks)

(iv) Explain when event rollover occurs in Timer3 and how it is indicated.

(3 marks)

(v) Explain the role of TMR3ON in Timer3.

(2 marks)

Q3 (a) Explain TWO (2) differences between asynchronous and synchronous data transmission.

(4 marks)

(b) State two serial communication modules in PIC18.

(2 marks)

(c) Given specification to transmit an 8-bit data using PIC18 EUSART with one Start and Stop bits in asynchronous mode. The data transmission speed is 9600 baud and the operating frequency for the PIC18 is 16MHz.

(i) Calculate the value to be loaded in the SPBRG register if the BRGH bit is cleared in the TXSTA register.

(4 marks)

(ii) Determine the byte value to be loaded in the TXSTA register.

(4 marks)

(iii) Write a C program to transmit a character "A" continuously.

(6 marks)

Q4 Devices can receive service from microcontroller through interrupt and polling methods.

(a) List THREE (3) types of interrupts available in PIC18 microcontroller.

(3 marks)

(b) Describe what interrupt priority is and why it is necessary.

(3 marks)

(c) With a single instruction, show how to disable all the interrupts.

(2 marks)

(d) Write instructions to setup INT1 with low priority and positive edge-triggered, Timer1 with high priority.

(7 marks)

(e) Create an ISR for Timer1 in **Q4(d)** to generate square waves on pin RC1.

(5 marks)

Q5 Answer the following questions by referring to the program in **Figure Q5**.

(a) Discuss FOUR (4) registers associated with EEPROM

(4 marks)

(b) State THREE (3) main functions of the program.

(6 marks)

(c) Determine the data size and baud rate of asynchronous mode serial transmission if the crystal frequency is 10MHz.

(3 marks)

(d) Explain the function for instruction ch=EE_READ( );

(2 marks)

(e) List all bits of the EECON1 that are used by the write operation of the EEPROM.

(3 marks)

(f) Explain the consequence when the instruction RCSTAbits.SPEN = 1 is changed to RCSTAbits.SPEN = 0.

(2 marks)

- END OF QUESTIONS -

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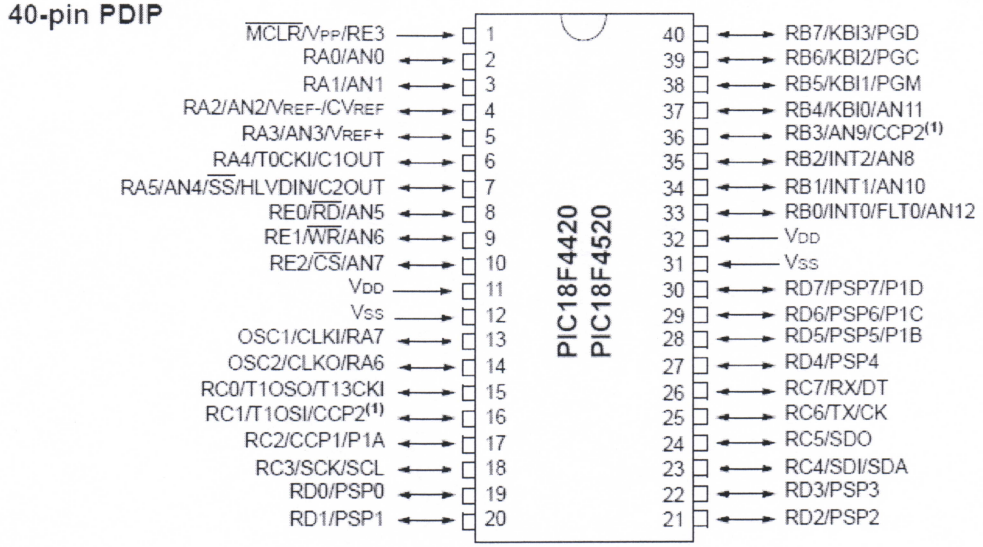

Figure Q1(a)

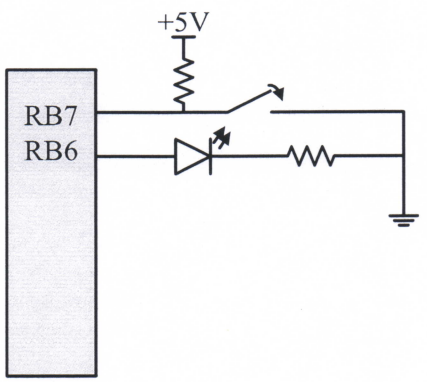

Figure Q1(b)

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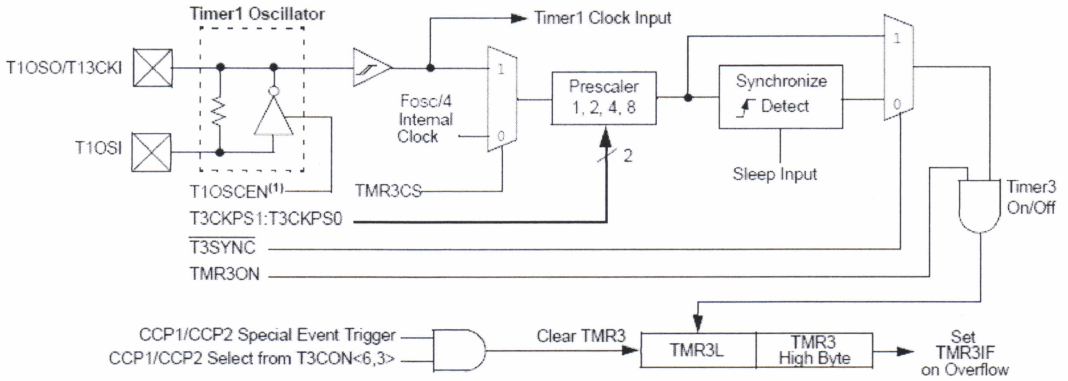

Note 1: When enable bit, T1OSCEN, is cleared, the inverter and feedback resistor are turned off to eliminate power drain.

Figure Q2(b)

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```
//Program Figure Q5
#include <p18f4520.h>
void EE_WRT(void);
unsigned char EE_READ(void);
void SerTx(unsigned char);

void main ( )
{
   rom far char* RomPointer="MOVE ME";
   char RamString[7];
   unsigned char x, ch, k=sizeof(RomPointer);
   TXSTA=0x20;
   SPBRG=15;
   TXSTAbits.TXEN=1;
   RCSTAbits.SPEN=1;

for (x=0;x<7;x++)     {
   RamString[x]=RomPointer[x];
   }

for (x=0;x<7;x++)     {
   EEADR=x;
   EEDATA=RamString[x];
   EE_WRT( );
   }
EECON1bits.WREN=0;

for (x=0;x<7;x++)     {
   EEADR=x;
   ch=EE_READ ( );
   SerTx(ch);
   }
   while(1)
}
```

Figure Q5

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```
void EE_WRT( )
{
   EECON1bits.EEPGD=0;
   EECON1bits.CFGS=0;
   EECON1bits.WREN=1;
   INTCONbits.GIE=0;
   EECON2=0x55;
   EECON2=0xAA;
   EECON1bits.WR=1;
   INTCONbits.GIE=1;
   while(!PIR2bits.EEIF);
   PIR2bits.EEIF=0;
}

unsigned char EE_READ ( )
{
   EECON1bits.EEPGD=0;
   EECON1bits.CFGS=0;
   EECON1bits.RD=1;
   return(EEDATA);
}

void SerTx(unsigned char c)
{
   while (PIR1bits.TXIF==0);
   TXREG=c;
}
```

Figure Q5 (continued)

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R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-1	R/W-0
CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D
bit 7							bit 0

CSRC: Clock Source Select bit

Asynchronous mode:
Don't care.

Synchronous mode:
1 = Master mode (clock generated internally from BRG)
0 = Slave mode (clock from external source)

TX9: 9-bit Transmit Enable bit

1 = Selects 9-bit transmission
0 = Selects 8-bit transmission

TXEN: Transmit Enable bit

1 = Transmit enabled
0 = Transmit disabled

Note: SREN/CREN overrides TXEN in Sync mode.

SYNC: EUSART Mode Select bit

1 = Synchronous mode
0 = Asynchronous mode

SENDB: Send Break Character bit

Asynchronous mode:
1 = Send Sync Break on next transmission (cleared by hardware upon completion)
0 = Sync Break transmission completed

Synchronous mode:
Don't care.

BRGH: High Baud Rate Select bit

Asynchronous mode:
1 = High speed
0 = Low speed

Synchronous mode:
Unused in this mode.

TRMT: Transmit Shift Register Status bit

1 = TSR empty
0 = TSR full

TX9D: 9th bit of Transmit Data

Can be address/data bit or a parity bit.

Figure 6: TXSTA (Transmit Status and Control Register)

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R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-x
SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D
bit 7							bit 0

SPEN: Serial Port Enable bit
1 = Serial port enabled (configures RX/DT and TX/CK pins as serial port pins)
0 = Serial port disabled (held in Reset)

RX9: 9-bit Receive Enable bit
1 = Selects 9-bit reception
0 = Selects 8-bit reception

SREN: Single Receive Enable bit
Asynchronous mode:
Don't care.
Synchronous mode – Master:
1 = Enables single receive
0 = Disables single receive
This bit is cleared after reception is complete.
Synchronous mode – Slave:
Don't care.

CREN: Continuous Receive Enable bit
Asynchronous mode:
1 = Enables receiver
0 = Disables receiver
Synchronous mode:
1 = Enables continuous receive until enable bit CREN is cleared (CREN overrides SREN)
0 = Disables continuous receive

ADDEN: Address Detect Enable bit
Asynchronous mode 9-bit (RX9 = 1):
1 = Enables address detection, enables interrupt and loads the receive buffer when RSR<8> is set
0 = Disables address detection, all bytes are received and ninth bit can be used as parity bit
Asynchronous mode 9-bit (RX9 = 0):
Don't care.

FERR: Framing Error bit
1 = Framing error (can be updated by reading RCREG register and receiving next valid byte)
0 = No framing error

OERR: Overrun Error bit
1 = Overrun error (can be cleared by clearing bit CREN)
0 = No overrun error

RX9D: 9th bit of Received Data
This can be address/data bit or a parity bit and must be calculated by user firmware.

Figure 7: RCSTA (Receive Status and Control Register)

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R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
PSPIF(1)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF
bit 7							bit 0

PSPIF: Parallel Slave Port Read/Write Interrupt Flag bit(1)
1 = A read or a write operation has taken place (must be cleared in software)
0 = No read or write has occurred

Note 1: This bit is unimplemented on 28-pin devices and will read as '0'.

ADIF: A/D Converter Interrupt Flag bit
1 = An A/D conversion completed (must be cleared in software)
0 = The A/D conversion is not complete

RCIF: EUSART Receive Interrupt Flag bit
1 = The EUSART receive buffer, RCREG, is full (cleared when RCREG is read)
0 = The EUSART receive buffer is empty

TXIF: EUSART Transmit Interrupt Flag bit
1 = The EUSART transmit buffer, TXREG, is empty (cleared when TXREG is written)
0 = The EUSART transmit buffer is full

SSPIF: Master Synchronous Serial Port Interrupt Flag bit
1 = The transmission/reception is complete (must be cleared in software)
0 = Waiting to transmit/receive

CCP1IF: CCP1 Interrupt Flag bit
Capture mode:
1 = A TMR1 register capture occurred (must be cleared in software)
0 = No TMR1 register capture occurred
Compare mode:
1 = A TMR1 register compare match occurred (must be cleared in software)
0 = No TMR1 register compare match occurred
PWM mode:
Unused in this mode.

TMR2IF: TMR2 to PR2 Match Interrupt Flag bit
1 = TMR2 to PR2 match occurred (must be cleared in software)
0 = No TMR2 to PR2 match occurred

TMR1IF: TMR1 Overflow Interrupt Flag bit
1 = TMR1 register overflowed (must be cleared in software)
0 = TMR1 register did not overflow

Figure 8: PIR1 (Peripheral Interrupt Request (Flag) Register 1

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R/W-x	R/W-x	U-0	R/W-0	R/W-x	R/W-0	R/S-0	R/S-0
EEPGD	CFGS	—	FREE	WRERR	WREN	WR	RD
bit 7							bit 0

EEPGD: Flash Program or Data EEPROM Memory Select bit
1 = Access Flash program memory
0 = Access data EEPROM memory

CFGS: Flash Program/Data EEPROM or Configuration Select bit
1 = Access Configuration registers
0 = Access Flash program or data EEPROM memory

Unimplemented: Read as '0'

FREE: Flash Row Erase Enable bit
1 = Erase the program memory row addressed by TBLPTR on the next WR command (cleared by completion of erase operation)
0 = Perform write only

WRERR: Flash Program/Data EEPROM Error Flag bit
1 = A write operation is prematurely terminated (any Reset during self-timed programming in normal operation, or an improper write attempt)
0 = The write operation completed

Note: When a WRERR occurs, the EEPGD and CFGS bits are not cleared. This allows tracing of the error condition.

WREN: Flash Program/Data EEPROM Write Enable bit
1 = Allows write cycles to Flash program/data EEPROM
0 = Inhibits write cycles to Flash program/data EEPROM

WR: Write Control bit
1 = Initiates a data EEPROM erase/write cycle or a program memory erase cycle or write cycle. (The operation is self-timed and the bit is cleared by hardware once write is complete. The WR bit can only be set (not cleared) in software.)
0 = Write cycle to the EEPROM is complete

RD: Read Control bit
1 = Initiates an EEPROM read (Read takes one cycle. RD is cleared in hardware. The RD bit can only be set (not cleared) in software. RD bit cannot be set when EEPGD = 1 or CFGS = 1.)
0 = Does not initiate an EEPROM read

Figure 9: EECON1 (EEPROM Control Register)

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R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF
bit 7							bit 0

GIE/GIEH: Global Interrupt Enable bit

When IPEN = 0:
1 = Enables all unmasked interrupts
0 = Disables all interrupts

When IPEN = 1:
1 = Enables all high priority interrupts
0 = Disables all interrupts

PEIE/GIEL: Peripheral Interrupt Enable bit

When IPEN = 0:
1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts

When IPEN = 1:
1 = Enables all low priority peripheral interrupts
0 = Disables all low priority peripheral interrupts

TMR0IE: TMR0 Overflow Interrupt Enable bit

1 = Enables the TMR0 overflow interrupt
0 = Disables the TMR0 overflow interrupt

INT0IE: INT0 External Interrupt Enable bit

1 = Enables the INT0 external interrupt
0 = Disables the INT0 external interrupt

RBIE: RB Port Change Interrupt Enable bit

1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

TMR0IF: TMR0 Overflow Interrupt Flag bit

1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

INT0IF: INT0 External Interrupt Flag bit

1 = The INT0 external interrupt occurred (must be cleared in software)
0 = The INT0 external interrupt did not occur

RBIF: RB Port Change Interrupt Flag bit

1 = At least one of the RB7:RB4 pins changed state (must be cleared in software)
0 = None of the RB7:RB4 pins have changed state

Note: A mismatch condition will continue to set this bit. Reading PORTB will end the mismatch condition and allow the bit to be cleared.

Figure 10: INTCON Register

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R/W-1	R/W-1	R/W-1	R/W-1	U-0	R/W-1	U-0	R/W-1
$\overline{\text{RBPU}}$	INTEDG0	INTEDG1	INTEDG2	—	TMR0IP	—	RBIP
bit 7							bit 0

$\overline{\text{RBPU}}$: PORTB Pull-up Enable bit
1 = All PORTB pull-ups are disabled
0 = PORTB pull-ups are enabled by individual port latch values

INTEDG0: External Interrupt 0 Edge Select bit
1 = Interrupt on rising edge
0 = Interrupt on falling edge

INTEDG1: External Interrupt 1 Edge Select bit
1 = Interrupt on rising edge
0 = Interrupt on falling edge

INTEDG2: External Interrupt 2 Edge Select bit
1 = Interrupt on rising edge
0 = Interrupt on falling edge

Unimplemented: Read as '0'

TMR0IP: TMR0 Overflow Interrupt Priority bit
1 = High priority
0 = Low priority

Unimplemented: Read as '0'

RBIP: RB Port Change Interrupt Priority bit
1 = High priority
0 = Low priority

Figure 11: INTCON2 Register

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R/W-1	R/W-1	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
INT2IP	INT1IP	—	INT2IE	INT1IE	—	INT2IF	INT1IF
bit 7							bit 0

INT2IP: INT2 External Interrupt Priority bit
1 = High priority
0 = Low priority

INT1IP: INT1 External Interrupt Priority bit
1 = High priority
0 = Low priority

Unimplemented: Read as '0'

INT2IE: INT2 External Interrupt Enable bit
1 = Enables the INT2 external interrupt
0 = Disables the INT2 external interrupt

INT1IE: INT1 External Interrupt Enable bit
1 = Enables the INT1 external interrupt
0 = Disables the INT1 external interrupt

Unimplemented: Read as '0'

INT2IF: INT2 External Interrupt Flag bit
1 = The INT2 external interrupt occurred (must be cleared in software)
0 = The INT2 external interrupt did not occur

INT1IF: INT1 External Interrupt Flag bit
1 = The INT1 external interrupt occurred (must be cleared in software)
0 = The INT1 external interrupt did not occur

Figure 12: INTCON3 Register