UTHM

Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER II
SESSION 2015/2016

COURSE NAME	:	VLSI DESIGN
COURSE CODE	:	BED 30303
PROGRAMME	:	BEJ
EXAMINATION DATE	:	JUNE / JULY 2016
DURATION	:	3 HOURS
INSTRUCTION	:	ANSWER **ALL** QUESTIONS

THIS QUESTION PAPER CONSISTS OF **SEVEN (7)** PAGES

Q1 (a) Timing Analysis, Extraction and Verification are among the steps in the VLSI design flow. Describe clearly each of these steps.

(6 marks)

(b) Analyse the stick diagram illustrated in **Figure Q1**.

(i) Draw the electrically equivalent transistor level schematic of the stick diagram.

(10 marks)

(ii) Deduce the logic equation for the output Y.

(4 marks)

Q2 (a) Find the output Y of the circuit shown in **Figure Q2** by analyzing which transistors on the circuit will be ON when the input $C = 0$, and then when the input $C = 1$. Determine the Boolean equation for the output Y.

(7 marks)

(b) Design a dynamic logic circuit with minimum number of transistors to realize the logic function of $F = \overline{WZ + X(Y + V)}$. The circuit must be able to eliminate a contention problem.

(8 marks)

(c) Construct a pass transistor circuit using only pMOS transistor to implement AND gate function.

(5 marks)

Q3 (a) Define logical effort in VLSI circuit design.

(2 marks)

(b) Calculate the logical effort for input A and B to the output for the circuit as shown in **Figure Q3(a)**.

(5 marks)

(c) In VLSI design, power consumption by the integrated circuit is always the main issues to be addressed by the designer besides the silicon area and speed or performance of the circuit.

(i) Discuss factors that contribute to the power consumption and loss due to the static and dynamic power.

(4 marks)

(ii) Propose and deliberate methods to minimize the power consumption.

(3 marks)

(d) Calculate the size for all PMOS transistors of the circuit illustrated in **Figure Q3(b)** such that the circuit will have an equivalent driving capability on an inverter. Given the minimum transistor length (L) is 2λ and the width (W) is 3λ; and the mobility of the electron is 3 times of the hole's mobility.

(6 marks)

Q4 (a) Edge-triggered flip-flop may experience hold-time failures or problems if the system has too much clock skew. State the meaning of clock skew and recommend **THREE (3)** techniques to eliminate or reduce these problems.

(5 marks)

(b) A positive-level sensitive (positive triggered) D latch circuit can be designed using a circuit as shown in **Figure Q4**.

(i) Examine and describe the operation of the circuit.

(4 marks)

(ii) Modify the circuit to produce a negative-level sensitive (negative triggered) D latch. Draw and clearly label the new circuit.

(3 marks)

(c) Design at full transistor level a negative edge or falling edge triggered D flip-flop using minimum number of transistors. Draw and completely label the circuit.

(8 marks)

Q5 (a) **Figure Q5(a)** is a 1-to-2 demultiplexer. Employ a pseudo-nMOS logic method to transform the circuit into a transistor level circuit with minimum number of transistors.

(4 marks)

(b) A block diagram of a 2-to-4 decoder is shown in **Figure Q5(b)**.

(i) Construct a truth table for the decoder and obtain the equation for each output.

(8 marks)

(ii) Design a dynamic 2-to-4 NOR decoder and draw the full circuit at transistor level with minimum number of transistors.

(8 marks)

– END OF QUESTIONS –

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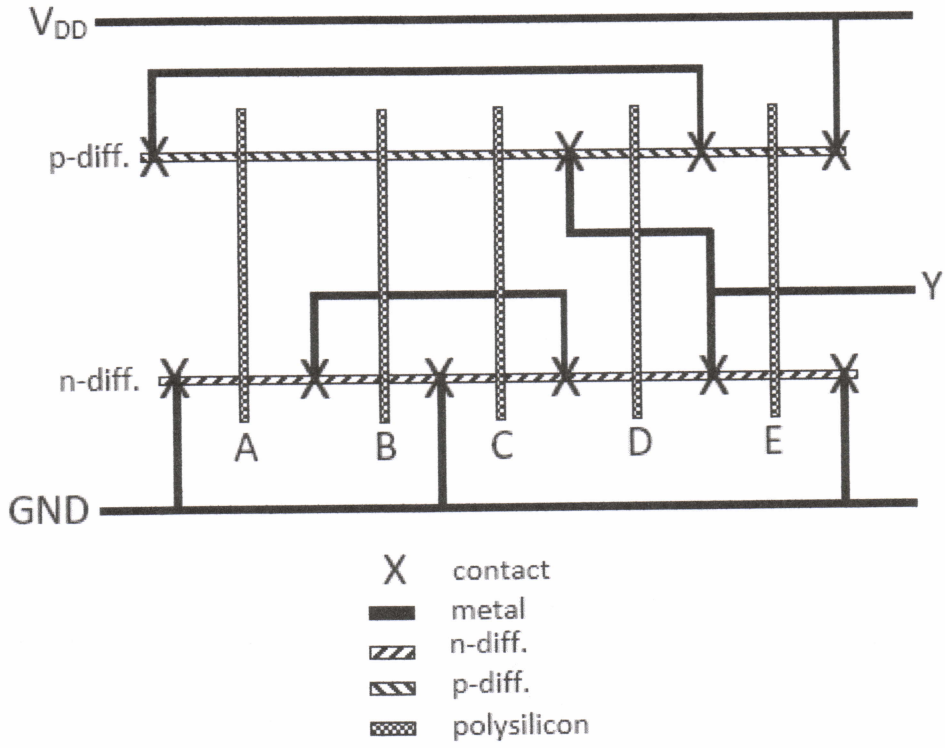

Figure Q1

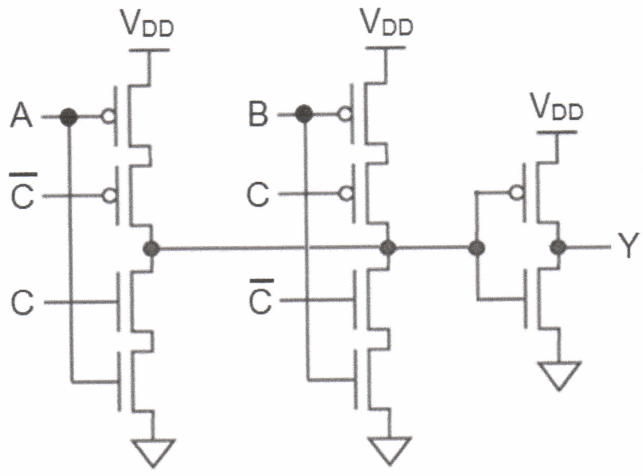

Figure Q2

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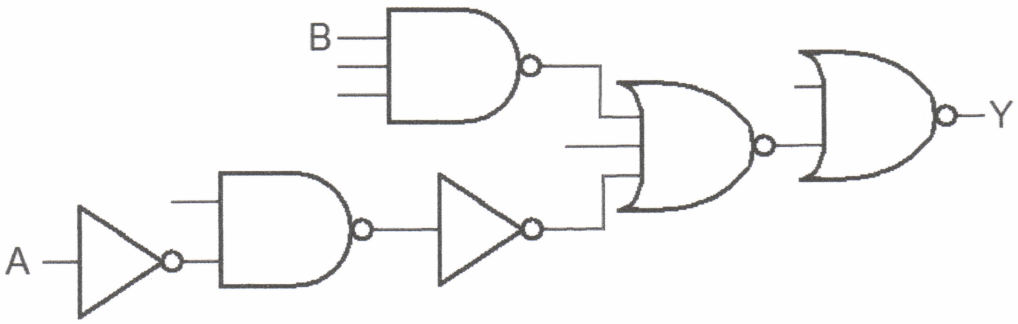

Figure Q3(a)

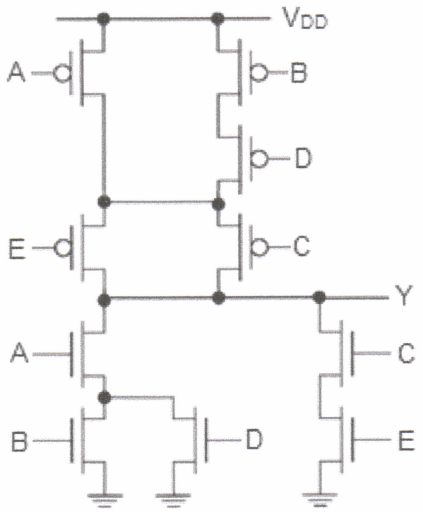

Figure Q3(b)

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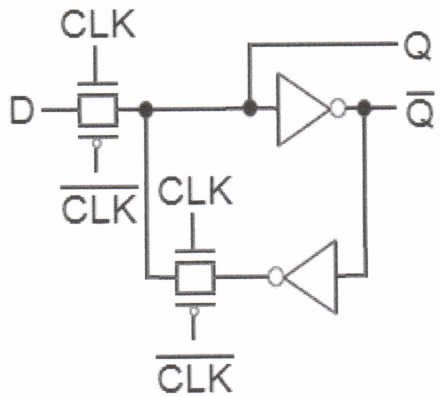

Figure Q4

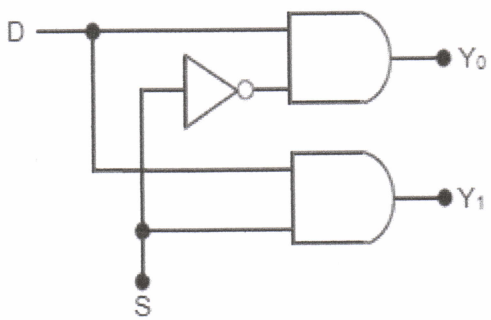

Figure Q5(a)

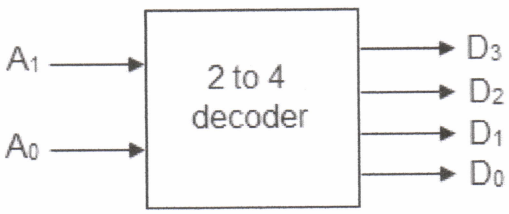

Figure Q5(b)