Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2015/2016

COURSE NAME	:	COMPUTER ARCHITECTURE AND ORGANIZATION
COURSE CODE	:	BEC 30303
PROGRAMME	:	BACHELOR OF ELECTRONIC ENGINEERING WITH HONOURS
EXAMINATION DATE	:	DECEMBER 2015 / JANUARY 2016
DURATION	:	2 HOURS 30 MINUTES
INSTRUCTION	:	ANSWER **ALL** QUESTIONS

THIS QUESTION PAPER CONSISTS OF **FIVE (5)** PAGES

Q1 (a) Convert the following expressions from Postfix notation to Infix notation.

(i) 3 5 7 + 2 1 − × 1 + +
(ii) ABCDE + F / + G − H / × +
(iii) 12 + 3 + 4 + 5 + 6 + 7 +

(3 marks)

(b) Convert the following expressions from Infix notation to Prefix notation.

(i) (5 × (4 + 3) × 2 − 6)
(ii) (A−B) × (((C − D × E) / F) / G) × H
(iii) (4 + 8) × (6 − 5) / ((3 − 2) × (2 + 2))

(3 marks)

(c) Produce a CISC-type program to evaluate the given arithmetic statement using:

$$S = \frac{A - E}{B \times C} + D / 6$$

(i) stack organized computer

(6 marks)

(ii) single accumulator

(6 marks)

(d) Consider a RISC-style processor, create a program that computes the expression Y = X3+Z* where Z = -A5*BC+ using three-address instruction format. Use only two registers in the program.

(7 marks)

Q2 (a) Processor, main memory, and I/O devices are interconnected by means of a bus and it provides a communication path for the transfer of data. Construct the complete I/O Module structure includes all the bus lines required.

(5 marks)

(b) A bus is a shared communication link that provides a communication path for the transfer of data. Give the advantages and disadvantages of bus lines as mentioned in Q2(a).

(5 marks)

(c) Explain with diagram for the function of I/O operation below as the processor sending/receiving data to the I/O device.

(i) Input Operation

(6 marks)

(ii) Output Operation

(9 marks)

Q3 (a) **Figure Q3(a)** shows a single bus organization of the data path inside a processor. Analyze the sequence of control steps required for the bus structure as shown for each of the following instructions. Assume that each instruction consists of two words.

(i) Subtract the content of register R1 with the content of register R3 into register R2.

(3 marks)

(ii) Multiply the number #3 with the result in Q3a(i) and save to register R1.

(2 marks)

(iii) Divide the content of register R3 with the sum of the #5 and the content of register R2, and save to register R1.

(4 marks)

(b) In the modern computer system, the use of multiple-bus organization is vital as market demand in high speed rate processor. Illustrate the diagram of multiple-bus organization with at least three data paths.

(7 marks)

(c) There are two phases in execute an instruction. Name them and explain the phases involves. Also includes the five-step sequence of actions to fetch and execute an instruction.

(9 marks)

Q4 (a) Pipelining is a technique of decomposing a sequential process into suboperations, with each subprocess being executed in a special dedicated segment that operates concurrently with all other segments. Illustrate a space time diagram for a three-segment pipeline showing the time it takes to process five-tasks, where the third task perform double the time to process.

(6 marks)

(b) Calculate the number of clock cycles that it takes to process 100 tasks in Q4(a). Assume that all tasks are performed in a single clock cycle.

(2 marks)

(c) A non-pipeline system takes 40 ns to process a task. The same task can be processed in a three-segment pipeline with a clock cycle of 12 ns. Produce:

(i) The speedup ratio of the pipeline for 80 tasks.

(2 marks)

(ii) The maximum speed up that can be achieved.

(2 marks)

Q5 (a) A computer system has a 8KB SRAM cache memory. Plan two (2) solutions to improve cache hit and cache latency.

(4 marks)

(b) For any given application running on a computer system with several levels of caches, set up two (2) techniques on how to increase the cache efficiency such that the overall computer performance can be increased?

(3 marks)

(c) Assuming that a computer system has the following memory properties:

Main memory:

Number of address lines: 10 bits
Number of input/output (data) lines: 64 bits

Cache memory:

Number of address lines: 15 bits
Number of input/output (data) lines: 64 bits
Number of words per block: 16

Based on the above specifications, determine the total number of bits for tag, block and word in the following scheme.

(i) Direct mapping scheme

(3 marks)

(ii) Associative mapping scheme

(3 marks)

- END OF QUESTIONS -

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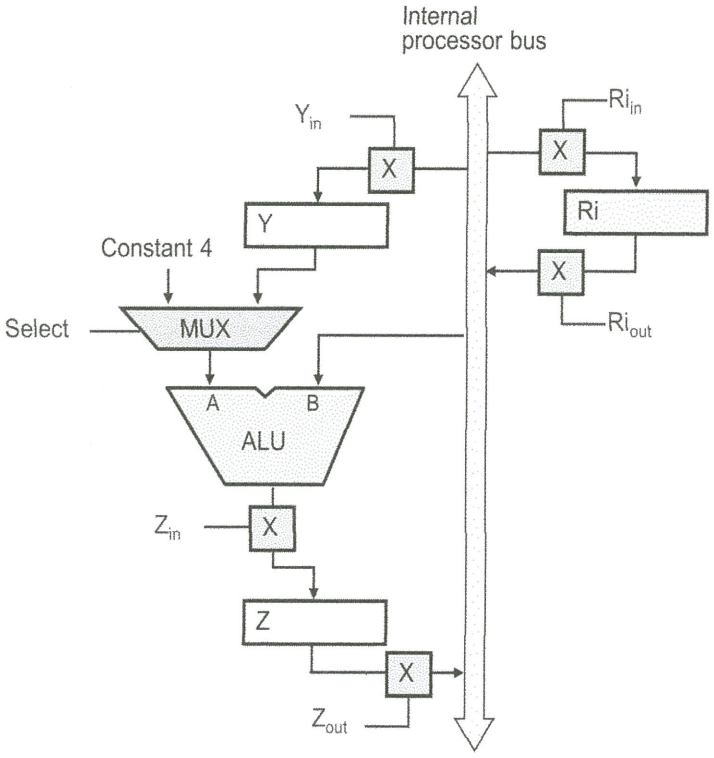

FIGURE Q3(a)