Universiti Tun Hussein Onn Malaysia

UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2015/2016

COURSE NAME	:	DIGITAL TECHNIQUES
COURSE CODE	:	BEF 12302
PROGRAMME	:	BACHELOR OF ELECTRICAL ENGINEERING WITH HONOURS
EXAMINATION DATE	:	DECEMBER 2015 / JANUARY 2016
DURATION	:	2 HOURS 30 MINUTES
INSTRUCTION	:	1. ANSWER **ALL** QUESTIONS
		2. ATTACH **APPENDIX A AND B** WITH YOUR ANSWER BOOKLET

THIS QUESTION PAPER CONSISTS OF **SEVEN (7)** PAGES

Q1 (a) Discuss the reasons why a digital system could not replace an analog system totally.

(3 marks)

(b) Convert BCD code 0110 0010 1001 to hexadecimal.

(6 marks)

(c) Convert the octal number 547 to Gray code.

(6 marks)

(d) The following minterm expansion is given, obtain a minimum Product-of-Sums (POS) expression.

$$F(A,B,C,D) = \sum m(0,2,3,4,8,9,10,11)$$

(5 marks)

(e) A NAND gate is a universal gate. Design the circuit to implement the following function by using only 2 input NAND gate

$$Z = \overline{A \cdot B \cdot C \cdot D}$$

(5 marks)

Q2 (a) By using Boolean theorem, prove that

$$\overline{X \cdot \overline{Y} + \overline{X} \cdot Y} = \overline{X} \cdot \overline{Y} + X \cdot Y$$

(3 marks)

(b) Digital systems must be able to handle both positive and negative numbers. A signed binary number consists of both sign and magnitude information. The sign indicates whether the number is positive or negative and while the magnitude is the value of the number.

Express the decimal number -15_{10} as an 8-bit binary number,

(i) in the sign-magnitude form. Show all the steps.

(3 marks)

(ii) in the 1's complement form. Show all the steps.

(2 marks)

(iii) in the 2's complement form. Show all the steps.

(3 marks)

(c) By using the 2's complement with 7-bit signed binary representation, subtract 15_{10} from $+50_{10}$. Perform the operation in binary.

(5 marks)

(d) Given the Boolean expression

$$P = (C + D).\overline{A.\overline{C}.D}.(\overline{A}.C + \overline{D})$$

(i) Obtain the minimum Sum of Product expression for P by using Karnaugh Map.

(5 marks)

(ii) Design the minimum combinational logic circuit for P.

(4 marks)

Q3 (a) Describe the operation of the following functional combinational logic circuit. You may use appropriate diagram and truth table to aid your explanation.

i) Decoder

(2 marks)

ii) Multiplexer

(2 marks)

(b) Implement the following Boolean expression using IC 74LS151 (8 line-to-1 line multiplexer) in **APPENDIX A**. Symbol for IC 74LS151 is shown in **APPENDIX A** for the internal circuitry and pins assignment of 74LS151 (8 line-to-1 line multiplexer).

$$Z = A \oplus B \oplus C$$

(6 marks)

(c) Implement the following Boolean expression using IC 74LS138 (3-to-8 decoder) in **APPENDIX B**. Symbol for IC 74LS138 is shown in **APPENDIX A** for the internal circuitry and pins assignment of 74LS138 (3-to-8 decoder).

$$f_1(x_2, x_1, x_0) = \sum m(0,1,5,6,7)$$

$$f_2(x_2, x_1, x_0) = \prod M(2,4,5)$$

(8 marks)

(d) Complete the missing entries (i), (ii), (iii), (iv), (v), (vi), (vii) and (viii) in **Table Q3(d)** of flip-flop excitation values required to produce the indicated flip-flop state changes. X indicates the present state and Y is the desired next state of the flip-flop.

(7 marks)

TABLE Q3(d)

Present state	Next State	J-K Flip flop		SC Flip flop		D Flip flop
X	Y	J	K	S	C	D
0	0	(i)	(ii)			(iii)
1	(iv)	1	1			
0	1			(vi)	(vii)	
1	(viii)	1	0			

Q4 (a) Explain **ONE (1)** advantage and **TWO (2)** disadvantages of a synchronous counter compared to an asynchronous counter.

(3 marks)

(b) A clock generator system input frequency is 36 kHz. The system is required to generate two frequencies, 9 kHz and 3 kHz at the outputs.

(i) In order to generate two output frequencies, two frequency divider circuits are required. Identify the MOD of counter for the two frequency divider circuit.

(4 marks)

(ii) Implement the two frequency divider circuit in **Q4(b)(i)** using IC 74LS293 (4-bit binary counter) in **APPENDIX C**. Symbol for IC 74LS293 is shown in **APPENDIX C** for the internal circuitry and pins assignment of 74LS293 (4-bit binary counter). You need to draw the circuit connection in your answer booklet.

(12 marks)

(c) Explain the operation of the Serial In Parallel Out (SIPO) register and Serial In Serial Out (SISO) register. You may use appropriate diagram to aid your explanation.

(6 marks)

-END OF QUESTION-

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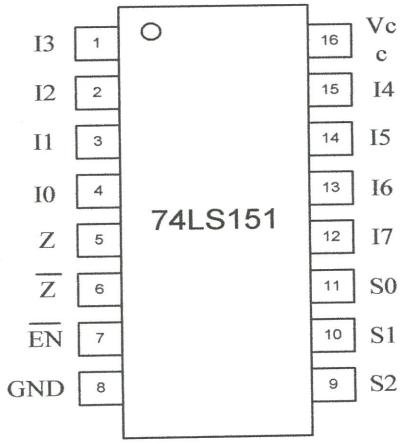
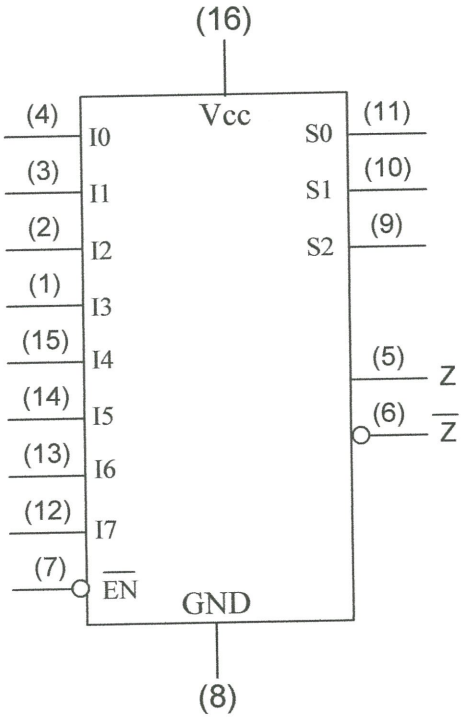
APPENDIX A

PIN ASSIGNMENT AND INTERNAL CIRCUITRY

74LS151 (8-to-1 Multiplexer)





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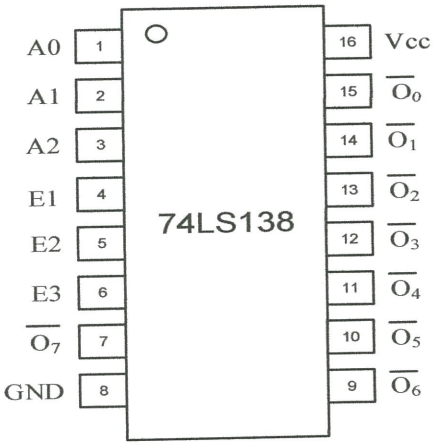
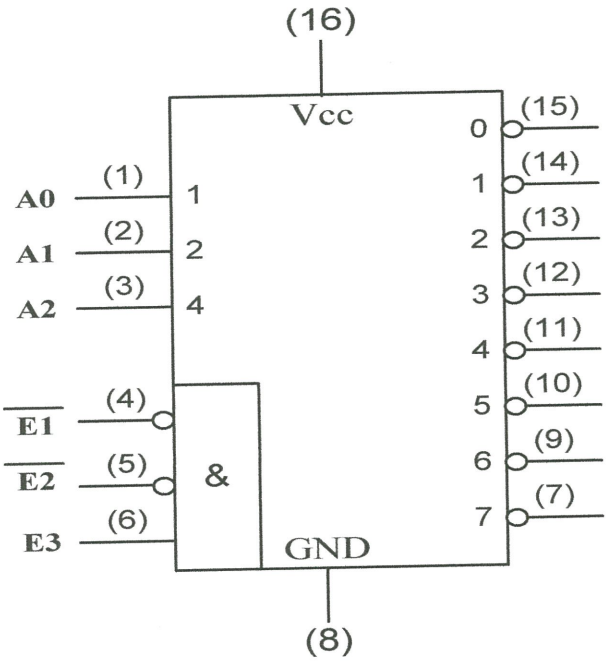
APPENDIX B

PIN ASSIGNMENT AND INTERNAL CIRCUITRY

74LS138 (3-to-8 Decoder)





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APPENDIX C

PIN ASSIGNMENT AND INTERNAL CIRCUITRY

74LS293 (4-bit binary counter)