UNIVERSITI TUN HUSSEIN ONN MALAYSIA

FINAL EXAMINATION
SEMESTER I
SESSION 2015/2016

COURSE NAME	: DIGITAL SYSTEM DESIGN
COURSE CODE	: BEC 30503
PROGRAMME	: BACHELOR OF ELECTRONIC ENGINEERING WITH HONOURS
EXAMINATION DATE	: DECEMBER 2015 / JANUARY 2016
DURATION	: 3 HOURS
INSTRUCTION	: ANSWER **ALL** QUESTIONS

THIS QUESTION PAPER CONSISTS OF **FOUR (4)** PAGES.

Q1 (a) State TWO (2) predominant hardware description languages.

(2 marks)

(b) Discuss a difference between FPGA devices and ASIC devices.

(2 marks)

(c) Sketch a typical design flow chart of CAD tools to implement a design into FPGA chip.

(6 marks)

(d) Briefly discuss the flow chart in **Q1(c).**

(10 marks)

Q2 **Figure Q2** shows a combination of three 2x1 multiplexers to create a 4x1 multiplexer.

(a) Clearly explain the difference between a structural HDL description and a behavioral HDL description.

(5 marks)

(b) Create a behavioral HDL description of a 2x1 multiplexer described in **Figure Q2**.

(5 marks)

(c) Create a structural HDL description of a 4x1 multiplexer that combines three 2x1 multiplexers in **Figure Q2**.

(10 marks)

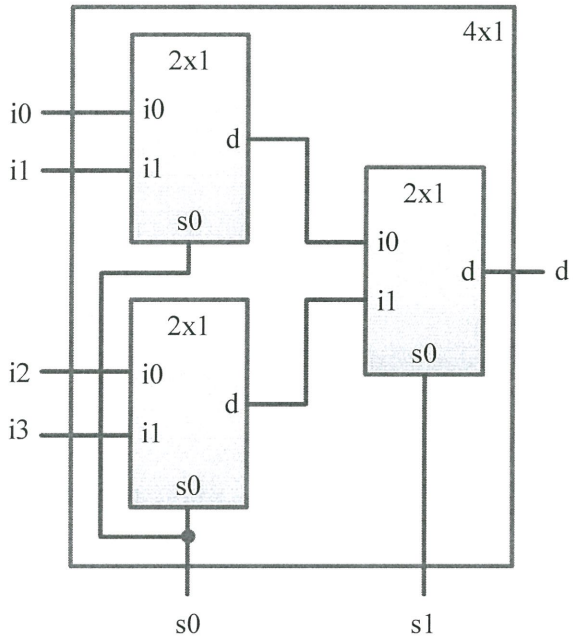

Figure Q2

Q3 **Table 3.1** lists the desired operations for a multifunction calculator to perform various basic Boolean operations.

TABLE 3.1: Desired operations.

Inputs			Operation
x	*y*	*z*	
0	0	0	S = A + B
0	0	1	S = A AND B (bitwise AND)
0	1	0	S = A NAND B (bitwise NAND)
0	1	1	S = A OR B (bitwise OR)
1	0	0	S = A NOR B (bitwise NOR)
1	0	1	S = A XOR B (bitwise XOR)
1	1	0	S = A XNOR (bitwise XNOR)
1	1	1	S = NOT A (bitwise complement)

(a) Create a block diagram for a multifunction calculator without using an arithmetic logic unit. The calculator has two 8-bit inputs *A* and *B*, and control inputs *x*, *y* and *z*.

(10 marks)

(b) Build a simple logic calculator using dual in-line package (DIP) switches for input and LEDs for output. The logic calculator should have three DIP switch inputs to select which logic operation to perform. A register is used to block output changes as the user configures the switches. The LEDs will display the value after a button *e* is pressed by user.

(4 marks)

(c) Explain and justify TWO (2) weaknesses of the design without arithmetic logic unit.

(6 marks)

Q4 Register-transfer level (RTL) design involves transferring data from registers, through other datapath components like adders, and back to register.

(a) Describe the steps of the RTL design process.

(8 marks)

(b) Create a datapath for the desired behavior to perform computations on input data shown in **Figure Q4**.

(12 marks)

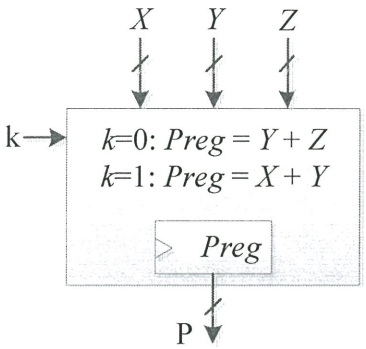

Figure Q4

Q5 (a) List all single faults in the circuit in **Figure Q5(a)** that can be detected using each of the test $w_1w_2w_3w_4 = 1100$ and 0110.

(8 marks)

(b) For the circuit shown in **Figure Q5(b)**, sensitize each path in this circuit to obtain a complete test set that comprises a minimum number of tests.

(13 marks)

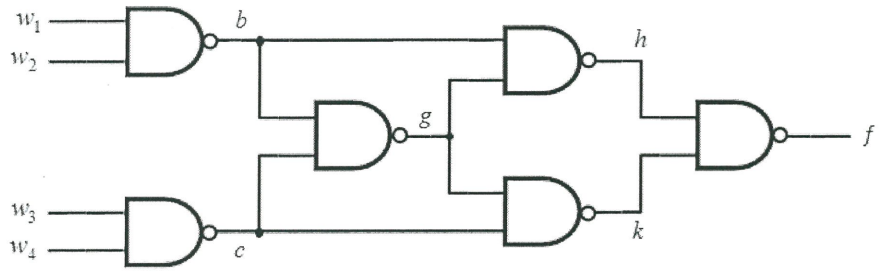

Figure Q5(a)

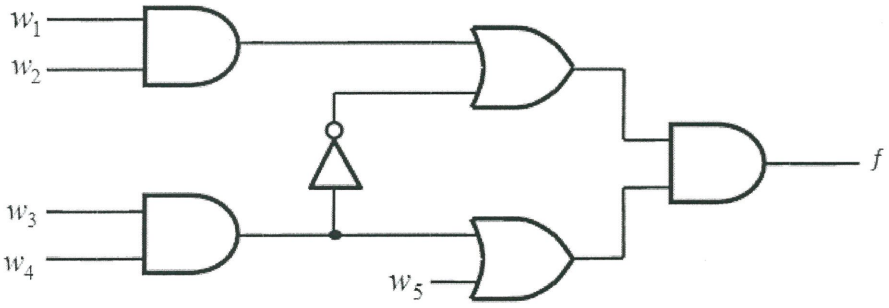

Figure Q5(b)

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